DESIGN AND DEMONSTRATION OF SIC 3D STACKED POWER MODULE WITH SUPERIOR ELECTRICAL PARASITICS AND THERMAL PERFORMANCES

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Haksun Lee

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Approved by:

Dr. Rao R. Tummala, Advisor
School of Electrical and Computer Engineering, School of Material Science and Engineering
Georgia Institute of Technology

Dr. Vanessa Smet, Co-Advisor
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Madhavan Swaminathan
School of Electrical and Computer Engineering, School of Material Science and Engineering
Georgia Institute of Technology

Dr. Yogendra Joshi
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Maryam Saeedifard
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Shyh-Chiang Shen
School of Electrical and Computer Engineering
Georgia Institute of Technology

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CHAPTER 1

STRATEGIC NEED, CHALLENGES, AND OBJECTIVES

1.1 Strategic Need

Environmental concerns have recently been driving stringent legislation to regulate and reduce automobiles' carbon emissions, with a worldwide target of 100g/km CO_2 emission by 2025, compared to the current 130g/km [1]. In an effort to comply with this regulation, the transportation industry has been pushing towards electrification of vehicles with various levels of electrification to choose, from micro, mild or full plug-in hybrid to all electric vehicles (HEVs and EVs). The percentage of cars that are electrified are increasing, and is expected to account for 25% of all cars, worldwide by 2025 [1]. An essential component of electric power is the power module that controls the energy flow. Electric cars are becoming more widely adopted with record sales in the last three years. The automotive power module market now accounts for about 42% of the total market for power modules and has been steadily driving innovations in this sector [2].

A typical power system architecture of an electric vehicle involves multiple power conversion stages, at different voltages and power ratings, as illustrated in Fig. 1.1. The power distribution starts with charging the high-voltage (HV) battery from the grid. The HV battery is charged through an on-board charger, a system that provides controlled AC-to-DC or DC-to-DC conversion of electric power to meet the charge profile of the battery. The HV battery provides power, not only to run the electric motor through the drivetrain inverter, but

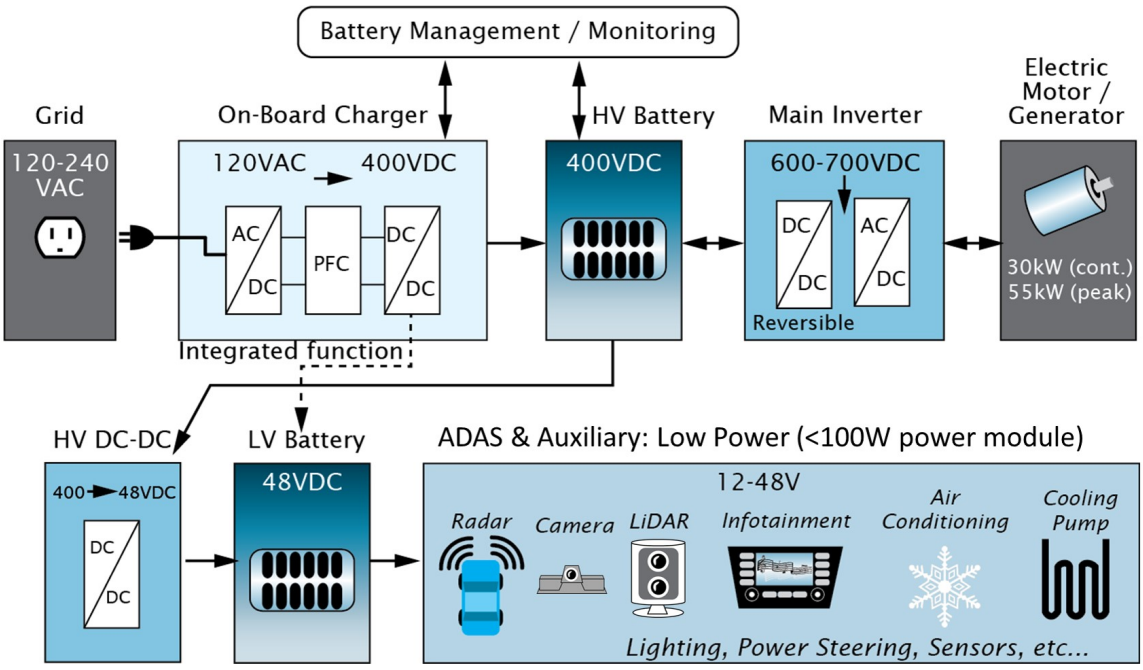


Figure 1.1: Power distribution and conversion of an electric vehicle

also to operate non-propulsion loads, such as advanced driver assistance systems (ADAS) and all auxiliary systems. Electric motors in (H)EVs typically operate by using a three-phase AC power source, wherein a drivetrain inverter draws power from a DC source (HV battery) and generates controlled AC waveforms to run the electric motor by use of power semiconductor switches.

Power semiconductor switches are essential for efficient power conversion, from source to load, by controlling and transmitting energy through their on/off switching. The most commonly-used semiconductor devices in EV drives currently are Si-based insulated-gate bipolar transistors (IGBTs), metal-oxide-semiconductor field-effect transistors (MOSFETs), and diodes. Unlike in microelectronics for data processing, these active devices comprise of a single component structure, either a single transistor or a diode, operating in vertical conduction to allow for increased current densities and breakdown voltages. An example

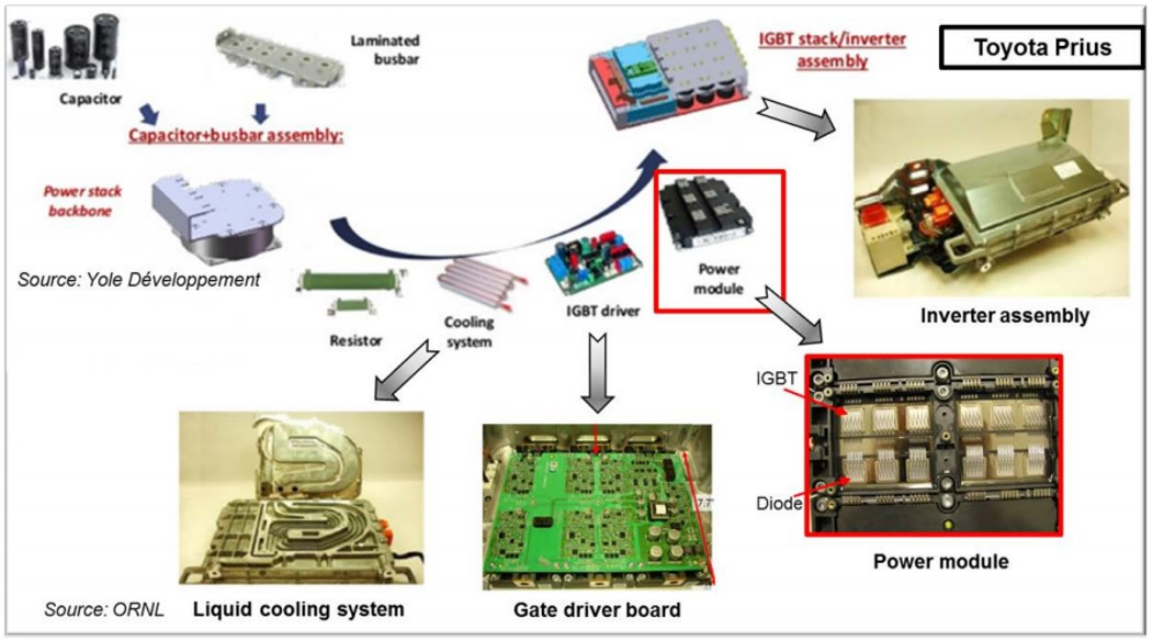


Figure 1.2: An example of automotive drivetrain inverter with all the component inside the inverter assembly including power modules (courtesy of Yole Developpement and Oak Ridge National Laboratory).

of drive-train inverter assembly with various components including passives, cooling system, control board, and conventional power module is shown in Fig. 1.2. Inside this power module, there are multiple semiconductor devices are co-integrated on a single substrate to realize a basic energy conversion function. In electric vehicle applications, the efficiency of the power conversion directly affects the performance of a vehicle such as the operating mileage range. Therefore, power modules are expected to play an increasingly important role in improving system performance. The selection of semiconductor devices, the way they are controlled, and how they are packaged, strongly impact the overall efficiency of EVs.

Like in all other electronics applications, performance improvements start with the device, its power ratings, breakdown voltage, operating temperatures and switching frequencies to reduce the size of the cooling systems. Silicon (Si) has traditionally been the mate-

rial of choice for power switching devices, primarily because of its manufacturability and relatively low cost. However, Si-based power devices have been reaching their limits in performance, design complexity, and cost [3, 4]. For instance, the blocking voltage and operating temperature of Si-IGBTs are limited to 6.5kV and 175^{o}C, respectively, and their switching frequency is relatively slow, limited to around 20kHz due to their high losses at increased frequencies [4, 5]. Higher breakdown voltage devices are desired, as they require less number of devices connected in series to block the voltage. On the other hand, higher operating temperature of power devices simplifies the cooling system with less stringent heat transfer requirements. To address these limitations and meet the ever-growing performance requirements of emerging power electronics, Silicon carbide (SiC), a wide-bandgap semiconductor material, has recently been identified and developed, as a promising candidate to replace Si. Devices made of Silicon Carbide (SiC) have advanced from preliminary laboratory prototypes to robust commercial products, over the last two decades, and are now considered a mature enough alternative to Si power devices, owing to their many compelling advantages, including higher breakdown voltages, higher operating electric fields, higher operating temperatures, higher switching frequencies, and lower switching and conduction power losses as summarized in Fig. 1.3 [4]. As a result SiC-based power electronics have been expected to bring significant volume reduction to the system.

For instance, the maximum junction temperature of power switches is determined by the intrinsic temperature at which the electrons in the valence band have sufficient thermal energy to move to the conduction band. This mode of conduction is uncontrolled and, therefore, undesirable in semiconductor power devices. In Si-IGBTs, this undesired phenomenon occurs around 150-175^{o}C, which sets the upper limit for operating temperatures

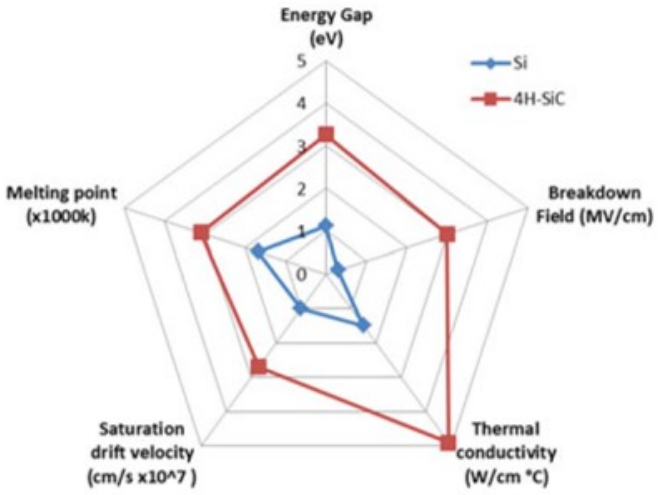


Figure 1.3: Material properties comparison between Si and SiC [4]

for Si power devices, while with SiC, it can be above 250°C. As a result, SiC devices are thereby projected to substantially reduce cooling requirements. Another advantage of SiC devices is their ability to operate at higher switching frequencies, which enables a significant reduction in the size of the passive components used in filtering. Despite their higher cost, as compared to their Si counterparts, SiC devices are expected to prevail in voltage ranges above 600V, because of the aforementioned system advantages they can bring to offset the increased device cost [3, 6]. As the typical voltage rating of the power devices in drivetrain inverters range from 600V to 1200V, SiC devices are particularly suitable for EV applications [4, 7, 8].

While rapid advances have been made with SiC device in their processing to improve performance, yield and manufacturability, the packaging of these devices has so far been limited to traditional such as wire bond. In such safety-critical applications as automobile driving, introduction of new technologies, particularly with respect to packaging, has been slow and incremental, rather than disruptive. Currently, SiC modules are packaged with

the traditional, and relatively low cost multi-chip module (MCM) approaches wherein the power devices are assembled on ceramic substrates with thick copper metallization, and interconnected through die-attach joints and bond wires for the bottom and top contacts, respectively [9]. However, this wire-bonded packaging approach, while robust, suffers from several drawbacks thus limiting the overall performance of the system: 1) high electrical parasitics, generating undesired power losses and noise that are further aggravated with faster switching SiC devices; 2)relatively high junction-to-ambient thermal resistance and too low thermal capacity thus, limiting both steady-state and transient heat dissipation performances; and 3) package materials and processes that are generally incompatible with high-junction temperature operations exceeding 200^{o}C, posing reliability concerns. These technical challenges are further discussed in the following section. To summarize, while significant advances in power semiconductor device technologies have been made, packaging is now the main limiting factor, preventing SiC-based power systems from fully achieving their performance and miniaturization potentials. Therefore, there is a very strategic need to explore and develop new generation of package designs, architectures, materials and processes, specifically designed for SiC-based power electronics.

1.2 Technical Challenges in Packaging of SiC Power Modules

1.2.1 Electrical challenges associated with increased switching speed of SiC power devices

One of the advantages of SiC devices is their fast-switching capability which can bring about a reduction in switching energy losses, and in size for the passive components, and, consequently, for the overall system. To illustrate this point, the turn-off characteristics of

a Si IGBT and a SiC MOSFET are compared in Fig. 1.4. It can be seen that the voltage (dv/dt) and current (di/dt) slopes are much greater for SiC MOSFETs than for Si-IGBTs; SiC devices turning on and off within a much shorter periode of time, and with a lower energy loss. Benefitting from these improved characteristics, SiC devices can, therefore, be switched at much higher frequencies (50kHz and higher) and with lower switching losses. At converter level, operating at higher switching frequencies leads to smaller energy storage requirements for passive components, and thus to a reduction in their volume and subsequent increase in power density for the overall system. However, these fast-transients of SiC devices create unwanted effects, when coupled with various parasitic elements that exist within the power module package, as illustrated in Fig. 1.5. The parasitic inductances (main switch loop and gate loop) are formed by the equivalent series inductance of conducting paths and interconnections such as, DC+/DC- bus, semiconductor devices, wire bonds, and gate terminals. Additionally, parasitic capacitances exist between the high-current contact on the top side of the insulating ceramic substrate and the ground terminal, which is usually at the bottom side conducting plane of the insulating substrate.

Further, the effect of the package parasitics, such as power loop inductance becomes more severe with fast-switching SiC devices, as compared to conventional Si-IGBTs. The high drain-current slope di/dt generated during the turn-off transients of SiC devices, adversely impacts the voltage waveform during their turn-off by causing the ringing and voltage overshoot. These undesired effects of the parasitic inductance result in increased switching energy losses. Since this energy loss occurs in every switching cycle, the switching frequency is often reduced as a result, which ends up limiting the overall system's performance and miniaturization. In other words, SiC devices have the capability to switch

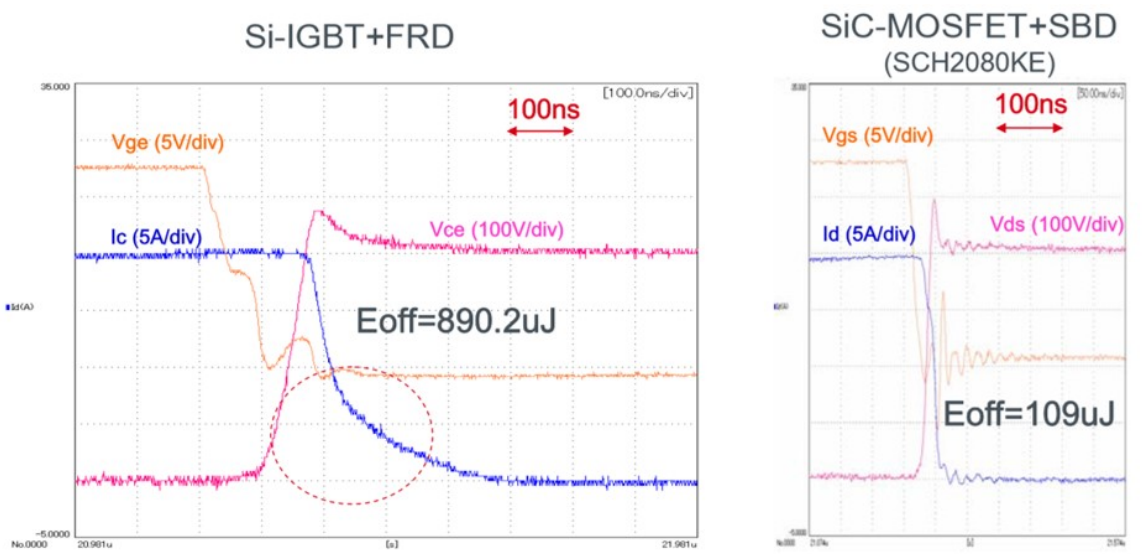


Figure 1.4: Turn-off switching waveforms of Si IGBT(left) and SiC MOSFET(right), showing different voltage and current slopes, where FRD stands for fast recovery diode, SBD for Schottky barrier diode, and Eoff is the energy loss at turn-off [5].

at faster speeds which lowers the switching losses, but the undesired effects of the parasitic inductance within the package deteriorate and restrict the benefits of fast-switching enabled by SiC devices.

These challenges of switching transients not only come from the current slope di/dt, but also from the voltage slope dv/dt. This dv/dt results in displacement currents through the

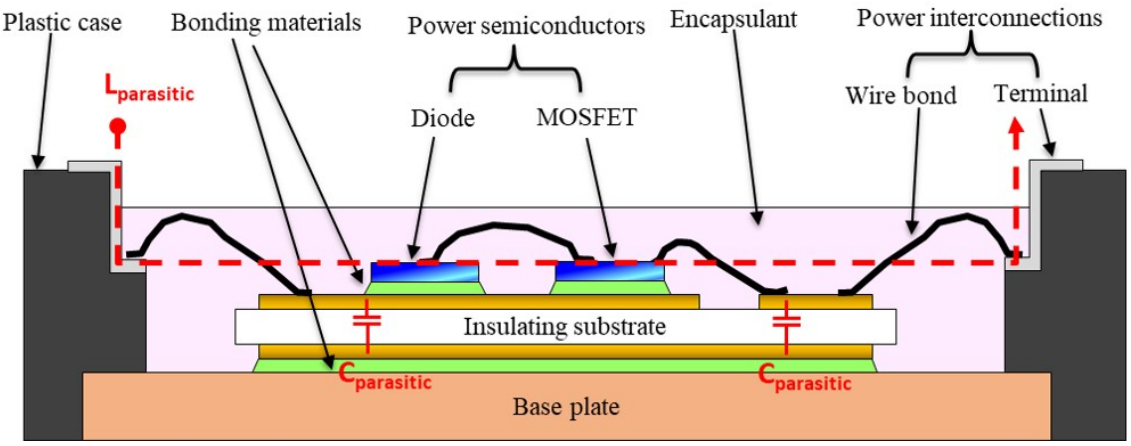


Figure 1.5: Parasitic elements that exist within the conventional power module package.

parasitic capacitance of the package, between the power devices and the cooling system. In conventional Si-based power modules, owing to the low dv/dt of Si devices, of around 3kV/μs, the current flowing through the parasitic capacitance was considered insignificant [10]. However, the dv/dt of SiC devices is more than an order of magnitude higher, up to 50kV/μs [10, 11], making the current flowing through the package capacitance no longer negligible. This undesired current can degrade the reliability of inverter-fed electrical machines [12] by generating, for instance, defects in the motor bearings by electrical discharge machining (EDM) [13]. Comparison studies on electromagnetic interference (EMI) of Si and SiC devices show that the conducted and radiated EMI increases with the use of SiC devices because of the faster switching speeds [12]. In addition to this undesired current flowing through the package into the cooling system, the capacitive parasitics are also responsible for slowing down the voltage transients, producing current overshoots during switching, and increasing EMI emission by forming resonant circuits with the parasitic inductances [14]. The current SiC power module packages based on the conventional direct-bonded copper (DBC) substrates have limitations in addressing this issue. Therefore, it is important to come up with novel package designs and materials that minimize the parasitic capacitance within the package and suppress the increased conducted and radiated EMI levels brought about by SiC devices.

In conclusion, the problems caused by fast transients, di/dt and dv/dt, should be addressed through novel packaging approaches that minimize both parasitic inductance and capacitance. Further, the impact of these parasitics on EMI should be carefully studied to identify which parasitic elements are significant contributors to the noise generation [15]

1.2.2 Emerging challenges associated with soft-switching converter topologies

An alternative approach to hard switching has been suggested to address the issues caused by fast switching transients from the converter topology standpoint. Soft switching converters are usually claimed to have reduced switching losses, better device utilization, reduced size of passive filtering elements, higher power density, and reduced EMI, which alleviates the difficulties with fast-switching transients [16, 17, 18, 19, 20, 21, 22]. These soft-switching converters targets to switch when the voltage (zero-voltage switching) and/or the current (zero-current switching) is zero to minimize switching losses, it is critical to precisely control the switching in near real time, which dramatically increases the complexity of the controller system design. Further, soft-switching topologies generally involve an additional number of power devices to control the resonance and create zero-voltage and zero-current switching conditions. Therefore, the effectiveness of soft switching should be assessed in relation to specific applications considering the additional complexity and cost from additional components, since it may not always offer the benefits mentioned above [22].

Current source-based converters using current switches, which consists of a switch and diode connected in series, are widely used in applications such as high-power industrial motor drives [23], renewable energies [24], and solid-state transformers (SST) [25, 26]. These current source converters are well suited for zero-current and zero-voltage based soft switching, and are predominantly employed with soft switching in the previously mentioned emerging applications [27]. The fast adoption of SiC devices is expected to scale up the voltage and power ratings, while further reducing the volume of these emerging

converters.

These current switch modules have an unconventional device configuration, in which a series diode is connected with a regular active switch to enable the reverse blocking. There are single die products called reverse-blocking IGBTs that does not require additional discrete diode connected in series to the switch as shown in Fig. 1.6(c). Except for these reverse blocking IGBTs, which have limited options of manufacturers, most researchers are forced to use series connected discrete switches to form a current switch [28]. In such an arrangement of discrete components, bond wires and bus bars create unwanted parasitic inductances in the circuit, which leads to increased turn-off duration and losses, and are usually considered as the primary cause of malfunctioning packages [28]. This packaging structure also comes with inherent challenges associated with high voltage stresses that are considerably larger than regular switches with the same ratings [27]. Thus, the package design of current switch modules requires an understanding of these unconventional challenges and accurate physics-based optimization accounting for the overall switch operation.

To summarize, the soft-switching topologies in combination with high-performance SiC devices can provide further reduction in losses, and therefore operate at higher frequencies, making the current switch modules an extremely competitive solution for emerging power electronic systems, going beyond conventional voltage source converter topologies. However, these new topologies can only reach their full potential if the inherent package challenges arising from these unconventional device configurations are fully addressed.

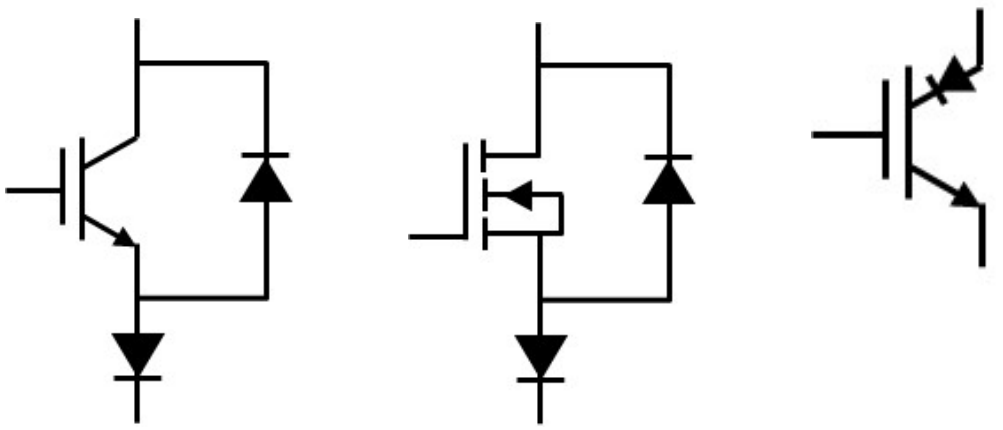


Figure 1.6: Possible options for current switches. (a) IGBT and diode, (b) MOSFET and diode, (c) Reverse–blocking IGBT.

1.2.3 Thermal challenges associated with high heat flux density of SiC power modules

Although present power devices convert power with acceptable efficiency, heat generation in these devices while they operate is unavoidable. Switching and conduction losses generated in the power devices create highly concentrated heat fluxes around the device and along the whole thermal path from chip to coolant [29]. Such heat fluxes cause perfor-

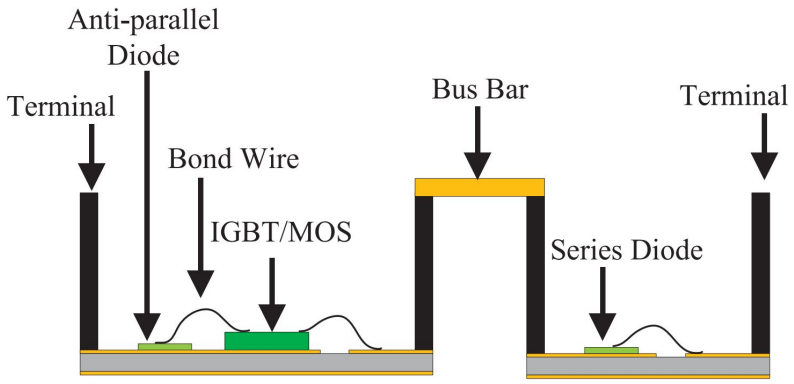


Figure 1.7: Package configuration for a current switch. Discrete modules are connected in series with a bus bar [28].

mance degradation in temperature-dependent device properties, such as increasing intrinsic carrier density, increasing junction leakage current, and reducing dielectric breakdown strength, in the power semiconductors, making them deviate from their ideal operating conditions. In addition, high heat fluxes aggravate thermally-induced reliability concerns at device and package levels.

To maintain acceptable maximum junction temperatures and temperature difference within the package (ΔT) in presence of active power cycling from the devices and passive thermal cycling from the environment, active thermal management approaches such as forced air convection or liquid cooling must be involved, which adds to the size, weight, cost, and complexity of the overall system. This load on the cooling system can be alleviated by the adoption of SiC devices, which can theoretically operate at junction temperatures greater than 250^{o}C.

One additional key feature of SiC devices is that they can be made in much smaller sizes than the Si devices for the same voltage and current ratings, which allows for more compact power module designs with higher power densities [14]. This increase in power density translates into higher thermal densities within the SiC modules. Power module packaging with SiC devices, therefore, requires more emphasis on heat spreading and cooling than with their Si counterparts. However, even combined with the most advanced cooling strategies such as direct base plate cooling using backside pin fin structures integrated into cold plates, the conventional power module packaging approach based on DBC substrates and wire bonds yields typical chip-area specific (junction-to-coolant) thermal resistances ranging from 0.3-0.4 Kcm^2/W, in typical 70kVA inverter systems [29]. Considering that the chip area is inversely proportional to the thermal resistance, the unit Kcm^2/W is used

to compare the thermal performance of different packaging approaches with different chip sizes. To meet the performance and cost targets of emerging power modules, this value needs to go below 0.2 Kcm^2/W, which can only be achieved with innovative approaches such as double-sided cooling [29].

The thermal design of power modules usually focuses on the steady-state performance, but the increased heat flux densities and faster power pulses brought about by SiC devices are now forcing designers to equally consider transient behaviors. Consequently, the thermal resistance should be minimized, whereas the thermal capacitance of the package needs to be maximized to reduce ΔTs resulting from these fast pulses [30].

In summary, power module packaging with SiC devices should consider higher heat flux densities that are expected with their smaller die sizes. Improvements in thermal resistance, heat spreading, and heat capacitance are needed to address the aggravated thermal challenges of SiC-based power electronics.

1.2.4 Reliability challenges associated with high-temperature operation

High-temperature power electronics that can function at ambient temperatures above 175°C without external cooling could greatly benefit a variety of applications such as automotive, aerospace, and energy production industries [30]. The fact that SiC devices are capable of operating at much higher temperatures, well beyond 250°C [9], [30], as compared to their Si counterparts has partially encouraged their development [30]. However, such high operating temperatures conversely affect reliability in two ways: 1) at material level, and 2) at a system level.

One of the biggest bottlenecks to enabling high-temperature SiC-based power electron-

ics is the lack of packaging materials capable of operating at such temperatures, above 200°C, without degrading the materials themselves or their interfaces with other materials. For instance, encapsulation materials used in power electronics are generally soft organic insulating materials designed for conventional Si power modules, and their normal range of operating temperatures is up to about 175°C–200°C [31]. There is limited understanding of the properties, in particular the electrical behavior, of such encapsulant materials at elevated temperatures and of their long-term aging performance [32]. Another critical class of materials are metals and alloys, commonly used as die-attach materials in conventional power module packages such as tin-based lead-free solders. The relatively low melting point T_m of these materials ($<$230°C) is a serious concern, preventing them from being used in high-temperature applications [33]. Indeed, when exposed to temperatures in excess to $0.5\times T_m$, these die-attach materials tend to aggressively form intermetallic phases, resulting in embrittlement of the joints, and aggravating reliability concerns. Also, the creep deformation becomes critical when the temperature exceeds $0.5\times T_m$ [34].

Secondly, the large thermal cycling loading that power modules experience creates mechanical stresses and strains in the different materials that the package is made of and at their interfaces due to the mismatch in their coefficients of thermal expansion (CTE) [30]. These thermal expansion stresses, particularly on the active dies, may cause a shift in their electrical performance (e.g. breakdown voltage and leakage current) to an unacceptable level, and should, therefore, be minimized [35, 36]. They also induce catastrophic fatigue-related failures with wire bond lift-off, cracking or delamination of the solder joints (die or substrate attach), and ratcheting of chip metallization on the top-side having been reported as the predominant failure modes in conventional power module packages [37, 38].

Table 1.1: Objectives, prior art, challenges, and tasks for the design and demonstration of 3D stacked SiC power module

	Parameter	Target	Prior Art	Challenges	Research Tasks
Electrical	Parasitic inductance	-20% reduction *	5.0 ~ 52 [nH]	**1. Trade-offs in multi-physics design** - High-speed switching - High thermal density - Heat spreading and stress **2. Vertical conduction methods** - Bulky fixtures - Complex process (ex. via drilling) - Limited conductor thickness	**1. 3D package design** - Low-parasitics L and C - Low-thermal resistance **2. Fabrication & Assembly of leadframe based compact 3D module** - Materials and process design - Simple stacking process **3. Characterization of 3D module** - Electrical (L, C, waveforms) - Thermal resistance
	Parasitic capacitance	-100% reduction *	75 ~ 140 [pF]		
Thermal & Mechanical	Thermal resistance	-20% reduction *	0.1 ~ 1.1 [°C/W]		

Increasing the device's junction temperature from 150°C to 200°C will further exacerbate the dominant failure mechanisms, and is expected to reduce the lifetime under thermal cycling by a factor of 50 based on available power module fatigue / creep degradation models, which is unacceptable in safety-critical applications such as automotive [14].

1.3 Research Objectives

The objectives of this research are to design and demonstrate a new class of ultra-low parasitics, 3D SiC power module for EV/HEV applications with high dv/dt capability, and enhanced thermal management and thermomechanical reliability, as detailed in Table 1.1. To achieve these objectives, it is essential to address the individual challenges that were previously mentioned. However, since these challenges are closely linked to each other, it is also critical to understand the trade-offs between the different physics that are coupled so as to optimize the power module design to best satisfy all below-mentioned objectives.

To realize the aforementioned objectives by addressing their corresponding challenges, three research tasks are undertaken: 1) concept design and demonstration of novel 3D package on full-bridge rectifier module, 2) low-inductance 3D SiC stacked half-bridge package

design, 3) modeling and design of multi-chip power module package for soft-switching current-switch module.

The first task consisted of a concept design of a novel 3D package design approach, demonstrating a simple full-bridge diode rectifier module as a proof-of-concept. The design was primarily focused on achieving low-parasitic inductance, low-parasitic capacitance, and low-thermal resistance with a new package architecture, with a module assembly process. The fabricated module was then characterized to extract its thermal and electrical performance characteristics, and these were then compared to the predictions of a finite element model (FEM) and benchmarked against wire-bonded and power card reference designs, respectively, to showcase the benefits of 3D integration.

The second task is aimed at extending this packaging approach to half-bridge module which is the most commonly used power module configuration in motor drive applications. Design considerations focusing on optimizing the package layout for thermal constraints, and minimizing the parasitics and their impact on the switching waveforms and noise generation, were studied and compared with to conventional packaging approaches.

Finally, the third task consisted of modeling and design of a multi-chip power module package for a soft-switching current switch module which is a unique circuit topology under evaluation for next generation soft-switching converters. A leadframe-based power card package was designed to meet module specifications that are relevant to EV applications. The design focus is to find optimum module footprint to trade-off between the thermal constraints, and low-inductance and symmetric layout package. A gate connection board was designed to make sure the paralleled devices were laid out with symmetry to prevent difference in switch timings of the devices. The proposed power card approach is

compared with a conventional power module packaging approach to verify improvements in thermal, electrical, and size aspects.

CHAPTER 2

PRIOR ART IN SIC POWER MODULES AND GT UNIQUE APPROACH

2.1 Current Industry Practice with SiC Power Packaging

Key milestones in the development of SiC power devices and their packages are highlighted in Fig. 2.1. The first SiC devices introduced to the market were Schottky diodes manufactured by Infi- neon in 2001. Since then, other companies like Cree and Rohm have continued to release SiC diodes with a variety of ratings. In 2008, SemiSouth produced the first SiC junction gate field-effect transistors (JFETs), and around that timeframe, companies started to integrate SiC Schottky diode bare dies into multichip power modules based on Si IGBTs, producing hybrid SiC power modules. From 2010 to 2011, Rohm and Cree introduced the first SiC metal oxide semiconductor field-effect transistors (MOSFETs) with a 1200V rating in discrete packages. As SiC power transistors became commercially available, companies such as Vincotech and Microsemi started producing full SiC modules using SiC JFETs and SiC diodes from 2011. In 2013, Cree introduced a fully SiC module using both SiC MOSFETs and diodes. Since then, other device vendors, including Mitsubishi, Semikron, Fuji, and In- fineon, themselves released all-SiC modules. In most cases, the SiC devices were first introduced as discrete components, and the implementation of those devices into a module package was developed after a few years following the initial device's release. One reason behind this is that the manufacturing process of discrete packages is by far much simpler than that of the power module package. The other

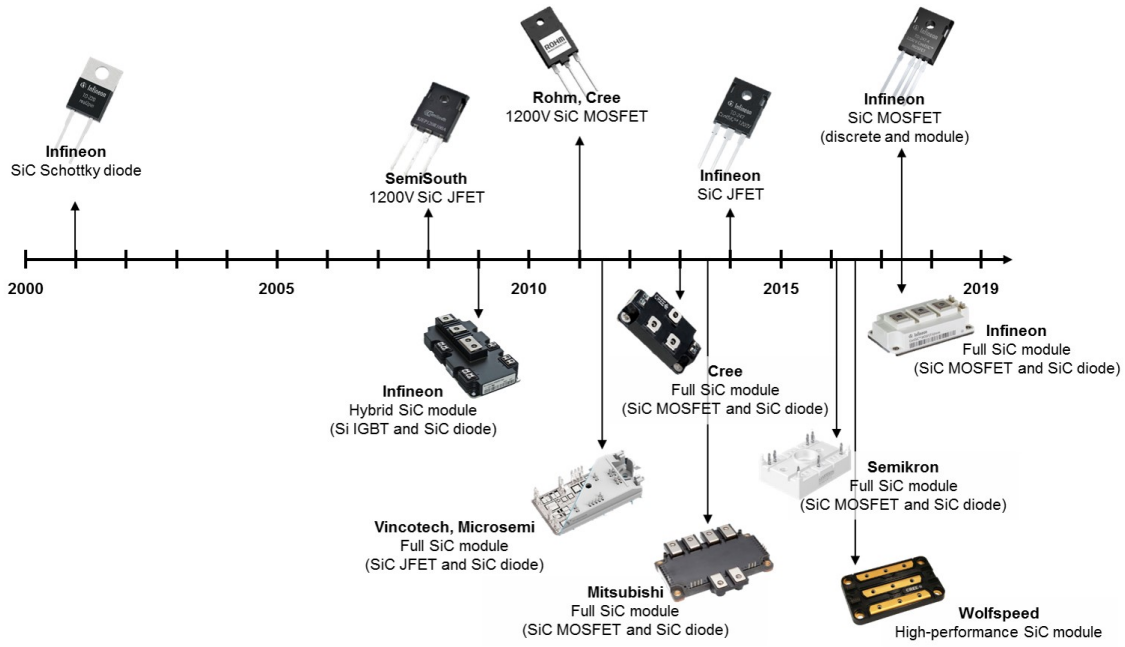


Figure 2.1: Development of SiC devices and their packages

reason, perhaps, is that the modules that are released have gone through extensive JEDEC standard qualification with a stringent power cycling reliability test, with over 20 million cycles without failures [39]. Discretely packaged devices have flexibility in designing energy conversion systems with lower cost, whereas the mod- ules benefit from increased performance and ease of integration and scalability once the products are readily available.

One thing to notice in Fig. 2.1 is that the newly developed devices are still packaged using conventional, albeit robust, packaging methods. To identify what efforts have been made to improve power module packaging over time, it is important to first understand the anatomy of a conven- tional power module. A conventional power module package consists of 7 basic elements, which are the power semiconductor chips, the insulating substrate, the base plate, bonding materials, power interconnections, encapsulating materials and a plastic case, as depicted in Fig. 2.2. These ele- ments in the module are composed of different classes of materials ranging from insulators, conduc- tors, and semiconductors to

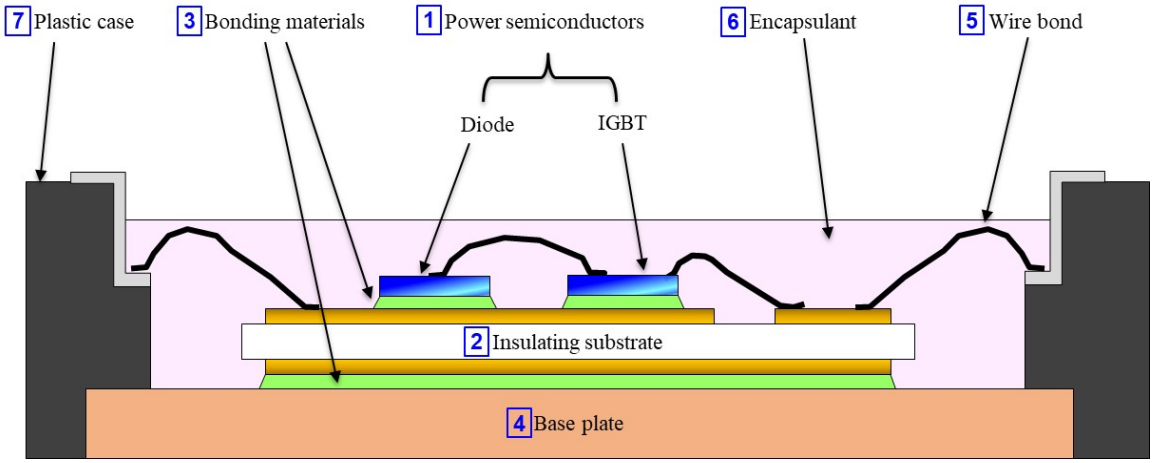
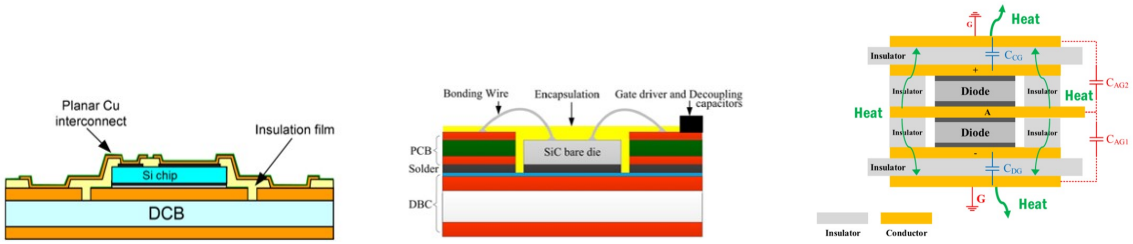


Figure 2.2: Cross-sectional diagram of a standard power module structure

organics and inorganics [40]. Since these different materials are strongly bonded together, it is critical to select proper materials for each element to form a robust and reliable package.

The manufacturing process for conventional power modules starts with soldering the power dies on a prepared DBC substrate using a vacuum reflow oven. Several of these DBC substrates with attached dies are then themselves soldered onto a base plate, using the same reflow process. The plastic case (excluding the cover) where the terminals are framed is mechanically attached to the same base plate with either glue or screws. Then the connections to the top side electrodes of the power dies, substrate metallizations, bus-bars and terminals are made through wire bonding, primarily using aluminum wires, as previously discussed. Lastly, the encapsulant material, typically a soft silicone gel, is deposited on top of the components with a dispenser, and the material is cured at an elevated temperature. The plastic cover is used in the finishing step to protect all the components within the package.



(a) (b) (c)

Figure 2.3: Advances in packaging for high-speed switching. (a) Planar interconnects [41], (b) Gate driver integrated hybrid packaging with integrated gate driver [42], (c)3D stacked power modules [15]

2.2 Recent Advances in SiC Power Modules and Key Innovations

Although most of the commercially available SiC devices are packaged using the standard method described above, there have been numerous efforts in the last decade to move away from this con- ventional approach and improve packaging technologies by addressing some of the challenges discussed in the previous sections. It is worth noting that many of these advances started even before SiC adoption became prominent, and are primarily applied to Si-based IGBT modules since the technical goals are common, but more stringent with SiC.

2.2.1 Advances in High-Speed Switching

To minimize the effect of the parasitic inductance of the main switching loop, elimination of lossy wire bonds, innovative 2D and 3D layout designs, and integration of periphery components such as bus bars with decoupling capacitors, have been suggested as detailed below.

Wire bonds require a certain loop height to form a reliable connection, as well as an extended footprint, larger than that of the die, for a wire to properly land on a conduc-

tor trace of the substrate. These result in lengthy interconnections which create relatively high parasitic inductances. Many inter- connection methods to replace wire bonds have been introduced. For instance, Fig. 2.3(a) shows a planar interconnect technology using direct deposited copper on the top-side of the power devices which reduces the loop area for the module current, yielding a 50% reduction in the stray inductance [41]. Similar planar interconnection methods, such as direct lead frame bonding [43], double-sided DBC integration [44], flexible PCBs [45, 46], and galvanic interconnections by direct copper plating [47], have been reported to provide a significant reduction in the parasitic inductance of the main switching loop.

Innovative 2D and 3D layout designs were considered to reduce the stray inductance as well. For instance, P-cell and N-cell based layout designs shorten the physical length of commutation loop [48]. Moreover, instead of the conventional layout configuration wherin utilizes power dies are all integrated in the X-Y plane facing upward, flipping some of the devices (downward facing) allows for current to flow in the X-Z plane which has a much lower enclosed area of the current loop [44, 49]. 3D stacking of power dies has also been proposed to even further minimize the issues related to di/dts. Placing one pair of power dies (a switch and a diode) on top of each other indeed creates a vertical current path with extremely low parasitic inductance within the package [50, 51, 52, 53].

Improvements in integration of the periphery components like bus bars and decou- pling capacitors was also proven to minimize the effect of parasitic inductances. Laminated bus bars cancel out the magnetic field by having opposite current paths [54]. Decoupling capacitors are brought closer to the module, or even embedded within the module, to nullify the effects of parasitic inductances from the terminals [54, 55].

Shortening the interconnection length between the power devices and their gate drivers will also reduce the gate loop inductances, which results in increased switching speeds. The first approach is based on conventional DBC substrates where the top-side of the package is integrated with a PCB board with cavities, and wire bonds are used to connect the gate driver ICs, capacitors, and power devices [56, 42]. Due to the inability of DBC substrates to incorporate low power components with fine features, power stage and drive circuitries have traditionally been integrated on separate PCBs, limiting the overall system's functional density [56]. However, this hybrid packaging method was proven effective in integrating heterogeneous devices and functions into a compact single package platform. A similar integration approach was demonstrated by Infineon [57]. Combining the lead frame and PCB structure, intelligent power modules integrate the driver ICs with the 3-phase inverter power stage, realizing a miniaturized system with enhanced functionality [57].

The second method is based on galvanic interconnections using a direct-plated via process [41, 58, 59, 60, 47]. In order to form these connections, the power dies and substrate are isolated using polymer dielectric layers, and vias are drilled directly on top of the devices' contact electrodes using a laser. The vias are then filled using a standard Cu electroplating process, forming Cu routing layers around 150um in thickness. In this approach, DBCs or lead frames can be used as base substrate. This method not only leverages existing power assembly technologies, but combines them with standard PCB manufacturing processes to realize a power embedding architecture.

To more directly address the EMI noise of SiC devices, active gate drivers have been invented. Different from previous methods which attempt to reduce the parasitics related to the gate driver interconnections, active gate drivers control the current and voltage slopes at

the turn-on and turn-off transients by adjusting gate resistance, gate source voltage and gate current. This active control of di/dt and dv/dt allows for enhanced switching behavior of the power devices by optimizing switching losses, reverse recovery current of the freewheeling diode, turn-off overvoltage, switching delay times, and electromagnetic interference [61, 62].

Different ways to control and suppress the common mode noise generated by dv/dts during switching have also been proposed, using customized gate drivers or filters. However, limited literature is available on reducing the effect of common mode noise through minimizing the parasitic capacitances of the power module package. In DBC substrates, the reduction of the overlapping area between the ground plane and a trace or plane that has potential fluctuations, has been suggested. By trimming the copper traces on the top-side of the DBC, the parasitic capacitance is minimized without affecting other layout parameters [63]. 3D power stacking structures also have been suggested to minimize the conducted EMI noise through the parasitic capacitance of the package. By placing the terminal which has the highest voltage fluctuations in the middle of a 3D sandwiched structure, drastic decrease in the parasitic capacitance between the terminal and the heat sink is achieved [51, 15]. While this approach looked promising from a modeling standpoint, manufacturability of the structures are questionable.

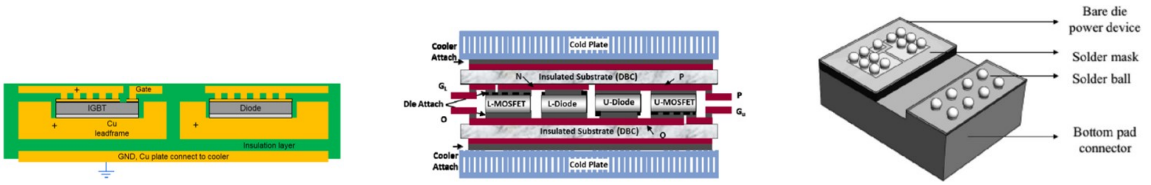
2.2.2 Advances in Thermal Management

Several alternatives to wire bonding have been introduced for top-side interconnection of the power dies to enhance the thermal dissipation of the package. For instance, an array of Cu posts can be soldered or sintered onto the die metallization for improved thermal

performance as in [64, 65], or wire bonds can be replace by large-area joints in a lead frame based implementation as shown in [66]. The latter type of bonding connects the whole metallization area of the die using either solder or sintered joints [67]. More recently, there has also been a noticeable increase in the implementation of electroplated vias to form the top-side interconnections [68, 59, 47]. This approach uses laser drilling of vias in dielectric layers covering the power devices, that are subsequently filled with Cu by electrodeposition to form the connections. These large-area contacts provide additional thermal paths contributing to the reduction of the thermal resistance of the package.

Several alternatives to wire bonding have been introduced for top-side interconnection of power dies to enhance the thermal dissipation of the package. Multiple of Cu posts are soldered or sintered onto the die metallization for improved thermal performances [64, 65]. Larger area joints are demonstrated using lead frames [66]. These types of bonding utilize the whole metallization area of the die using either solder or sintered joints [67]. More recently, there has been a noticeable increase in the implementation of electroplated vias to form the top-side interconnections [68, 59, 47]. These approaches use laser drilling of vias on dielectric layers, and fill them up with Cu with electroplating process to form the connections. These large area contacts provide additional thermal path contributing to the reduction of thermal resistance of the package.

Fig. 2.4(a) shows a thick lead frame structure which appears in many of the recent power module package solutions as a bottom substrate [47]. This thick (1.5mm) lead frame substrate, which is usually made of copper, spreads heat effectively before it reaches the insulation layers. It also simplifies and eliminates a number of the package layers, such as the heat spreader and solder substrate attach, resulting in reduced junction-to-case



(a) (b) (c)

Figure 2.4: Advances in packaging for enhanced thermal management. (a) Thick lead frame as a substrates [47], (b) Double-sided cooling with DBC substrates on top and bottom [44], (c)Wire bonless 3D flip-chip package [69].

thermal resistance[49, 70, 43].

Popular double-sided cooling approaches have DBCs or other substrates on both top and bottom side of the module as shown in Fig. 2.4(b). Increased contact area on both sides of the die allows for more uniform temperature distribu- tion of the structure, reducing the peak temperature as well as the overall package thermal resistance [44, 54, 71, 72, 73]. More recently, a chip-scale package was suggested as an alternative way to achieve double-sided cooling (Fig. 2.4(c)). A power die is assembled on a metal- lic connector with solder balls, and then flip-chip bonded onto a substrate, allowing heat dissipation from both sides of the device [69].

2.2.3 Advances in Thermomechanical Reliability

Die-attach materials proven for standard Si-based modules temperature range (150°C–175°C) have low glass transition temperature that are not suitable for high-temperature operation of SiC-based modules. Moreover, a special attention needs to be paid to matching the CTE of die, die-attach, and substrate and reduce thermal expansion stresses and strains. Many alternatives to conventional Sn-rich solders have been proposed to be implemented in future SiC power modules, considering these two criteria [74]. Gold-based solder materials, such as

AuSn eutectic, have gained popularity fort their high-temperature performance (>280°C), high electrical and thermal conductivity, and easy fluxless soldering [75]. However, they are only suitable for small die applications be- cause of their increased stiffness and high cost. A two-step fluxless bonding process using a silver-indium alloy has also been suggested for high-temperature die-attachment [76]. This process is also a fluxless bonding method, but benefits from a low process temperature (206°C) and high re-melting at around 780°C, making it a viable alternative for a high-temperature and reliable die-attach material. Many other TLP (transient liquid phase) or SLID (solid- liquid interdiffusion) systems have also been explored to provide solutions that satisfy the requirements of SiC modules at a relatively lower cost [77]. A more expensive SLID bonding approach us- ing AuSn was also demonstrated [61], and showed great potential in high-power and high-reliability die-attach applications [78].

Silver sintering is also a bonding method renowned for its low temperature processing (¿220°C) and high melting point (961°C), with many other advantages such as superior thermal con- ductivity and enhanced reliability in thermal and power cycling [79, 80]. There still are challenges, however, to be solved, primarily related to complicated and costly assembly processes that come with the need for dynamically-controlled applied pressures in bonding and customized surface metallizations, along with reliability concerns from, for instance, entrapment of volatiles with large dies. More recently, sintering interconnections based on nano-copper materials are being researched as a lower cost alternative and to address the migration issues experiences with Silver [81, 82]. The demonstration of organics-free nano-copper sintered die-attach shows improved manufacturability as compared to traditional nanopaste or film approaches, with added design flexibility for stress

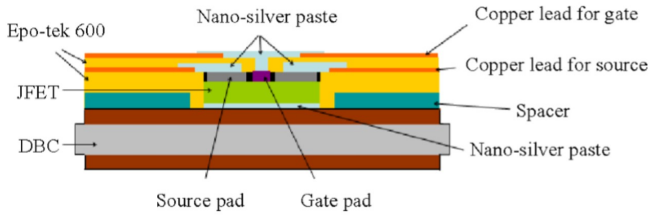


Figure 2.5: Demonstration of high-temperature SiC power module [85].

management, making it a promising alternative for high-temperature die-attachment of SiC devices [82].

With respect to encapsulation materials, several types of polymers were considered for high-temperature operations [83]. Candidates that have glass transition temperatures (Tg) higher than 250°C include polyimide, Benzocyclobutene, Silicone elastomer among others [83, 32]. Namics developed a new resin technology with high thermo-stability for SiC power module applications [84]. Their innovative formulation incorporates high thermal conductivity fillers, granting this new encap- sulant material a high Tg of 293°C, and showing improved performance in high-temperature aging tests [84].

Actual operation of SiC module packages under high-temperature conditions was also demonstrated in [85, 86]. The SiC JFETs and SiC diodes are packaged on a DBC, as shown in Fig. 2.5, and the top-side connections are made by applying multiple layers of polyimide and nano-silver paste for electrical isolation and connections, respectively. Under ambient temperature of 250°C, I-V characterization of the packaged SiC dies was conducted, along with re- liability assessments such as high-temperature storage and thermal cycling with a maximum temperature of 250°C [85]. Other research activities involving gate drivers in high-temperature operation were presented in [87, 88, 89], wherein a SiC MOSFET module with integrated SOI (silicon-on-insulator) gate drivers showed capability to operate at up

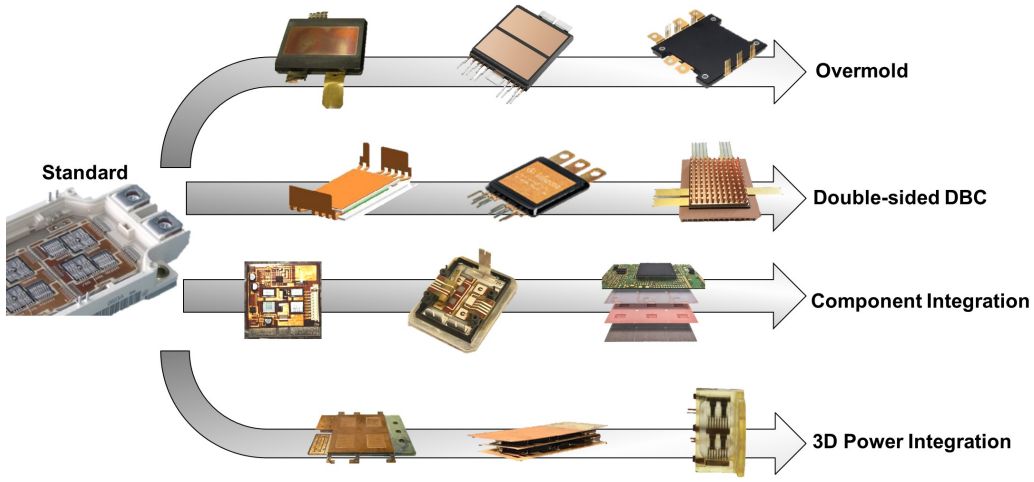


Figure 2.6: Advances in packaging structures. Overmold structures show compact and flat form factor which strengthens the modularity [90, 43, 91]. Double-sided DBC structures allow heat dissipation from both top and bottom side of the module [71, 72, 92]. Component integration structures combine heterogeneous functions into the module to enable fast-switching [93, 45, 94]. 3D power integration structures have power dies stacked in vertical direction which alleviates the di/dt and dv/dt issues [53, 50, 52]

to 200°C. The materials used to build this SiC power module, as well as the components utilized for the gate drivers and passives were carefully selected based on their maximum temperature ratings.

2.2.4 Major Trends in Power Module Designs

Innovative package structures and designs have been derived from standard power modules. While some examples show only minimal – incremental - changes in the packaging elements, their impact on the overall package performance is not trivial. Although it is difficult to group them, recent advancements in package designs are classified into four categories, based on their similarity in module structure and design purpose. Fig. 2.6 presents the evolution in each category, which are as follows: overmold, double-sided DBC, component integration, and 3D power integration.

The overmold structures are lead-frame based power modules where power dies are directly attached to the lead frames, and overmolded with epoxy molding compounds. The wire bonds on the top-side of the dies for power terminals are replaced with lead frames bonded with solder, forming larger area joints. In most of the existing overmold structures, however, the gate terminals are still connected using wire bonds. Studies on overmold structures demonstrated a drop in the package internal inductance, a decrease in the power loss, improvements in thermal resistance, and longer power and temperature cycling lifetimes [49, 70, 43] as com- pared to the standard designs. The reduction in inductance and power loss is attributed to the flat and short electrical length and arrangement of the lead frame interconnections. Con- sidering the top-side heat spreading in addition to the conventional bottom-side one, the thermal resistance of this structure is significantly decreased compared to that with standard alumina-based DBC substrates. The increased contact area between die and lead frame also allows for more uniform temperature dis- tribution in the structure, reducing the junction peak temperature, and, consequently, the induced stress on the dies. This reduction in mechanical stresses is reflected in the improvement in lifetime under power cycling conditions [70].

One remarkable advantage of the overmold structure is the enhanced modularity and ease of scalability in power range. These structures usually come with thinner profiles, reduced footprint, and low weight. Converters using multiple of these repetitive structures simply by stacking them were found to benefit from dra- matic improvements in power density of the system, including the cooling management [95]. Volume and weight constrained applications such as EVs/HEVs would benefit the most from overmold structures with such enhanced modularity.

The double-sided DBC structure shares very similar features with the overmold structure. The removal of wire bond offers very low package inductance and a reduction in thermal resistance, enabled by double-sided cooling. In order to compensate for the different thicknesses of the dies and respect isolation distances between the terminals, metal posts are often inserted between the die and the top-side DBC. The advantages of double-sided DBC structures over standard modules include low loss, improved thermal performance, and cost-effective manufacturing [44, 54, 71, 72, 73].

The component integration structures aim to combine multiple functional components into a single package module. The main motivation of this structure is to integrate gate driver ICs and/or decoupling capacitors with the power devices in a compact module, and, thereby, enable faster switching performance. As previously mentioned, shortening the interconnection length between power devices and their gate drivers brings a reduction in the gate loop inductance, which in turns results in increased switching speeds. Moreover, decoupling capacitors can cancel out the effect of parasitic inductances from bus bars or external connectors. Thus, it is highly desirable to package these components as close as possible to the power dies for efficient power conversion.

The 3D power integration structures go one step further in improving the package integration density to solve the fast-switching transient issues. This unique configuration takes advantage of the third dimension, shortening the interconnection length of the main switch loop, and shows extremely low parasitic inductance. The output terminal, which is the main source of conducted EMI noise, is placed in between the positive and negative terminals, isolated from the heatsinks that are electrically grounded. This configuration eliminates a direct path for the common mode currents to flow, resulting in minimizing the dv/dt issue

caused by the parasitic capacitance that exists in conventional DBC-based packages [51]. Combining components other than power dies such as decoupling capacitors [50], gate drive ICs [52], and heatsinks [53] into the 3D module has also been demonstrated, which shows capability to incorporate heterogeneous functions into the package. Due to the challenges in maintaining the temperature uniformity of the module, studies emphasized the need for increased thickness of the conducting layer [50], or increased heat capacity of the module [53], for improved thermal performance.

2.3 GT PRC's Unique Approach

The unique approaches to address the challenges mentioned in Chapter 1 are shown in Fig. 2.7. The proposed package is a leadframe based 3D package, where the power devices are stacked in vertical direction with sintered die attach joints. The uniqueness of the package can be explained by three main benefits of the 3D package, namely, electrical benefits, thermal benefits, and manufacturing benefits.

The power loop inductance is minimized by utilizing the xz-plane interconnections instead of xy-plane. Recent developments on planar interconnect approaches successfully replaced conventional wire bond technology by reducing the footprint, reducing parasitic L and R, and improving reliability. However, the power loop (a current path from positive voltage source through the module package, and back to to negative voltage source) is laid out on 2D xy-plane creating large loop area, and resulting in non-negligible stray inductance of the package. This stray inductance can further be minimized by making the loop through xz-plane (vertical direction) leveraging the short connection length from the bottom side to the top side of the package. In addition, the power loop inductance can fur-

ther be minimized by terminal bus bar designs. The terminal bus bars often are the biggest contributors to the parasitic inductance since they are usually long conducting path which connect the power source to the power module. Different from conventional terminal structures, the proposed 3D structure have positive and negative terminal on top of each other. This structure where the conductors are aligned to face each other and the current flows in opposite direction, cancels out the magnetic field and therefore reduces the inductance associated with the terminals.

The impact of dv/dt will be addressed by minimizing the package parasitic capacitance of the package. As the noise generating terminal with the highest potential fluctuation is the output terminal which is positioned in the middle leadframe layer, the noise current has no direct path to flow to the heatsink, preventing it to circulate to other systems. The material and dimensions of the isolation layer (thin film dielectric) of the package will give flexibility in optimizing parasitic capacitance.

The proposed power module has three elements that drastically reduce the thermal resistance of package compared to conventional structures. Firstly, the top and bottom thick leadframes act as Cu heat spreaders, immediately dissipating the heat generated from the semiconductors. Secondly, the large area joints on both sides of power devices with high-thermal conductivity sintered die attach allows additional reduction in thermal resistance of the package. Thirdly, the double-sided cooling structure greatly reduces the thermal resistance from junction to case. The generated heat is transferred through bottom (junction-to-bottom) and top (junction-to-top) heat spreader that are in parallel resulting in significant reduction in equivalent thermal resistance of junction to case.

The proposed assembly approach is a low-cost leadframe and overmold based pro-

cesses which are both compatible with existing fabrication infrastructures which do not require customized equipment or environment. Unlike other 3D approaches, the proposed assembly does not involve complex processes to form vertical joints, such as via drilling and plating, or bulky fixture structures to press the package.

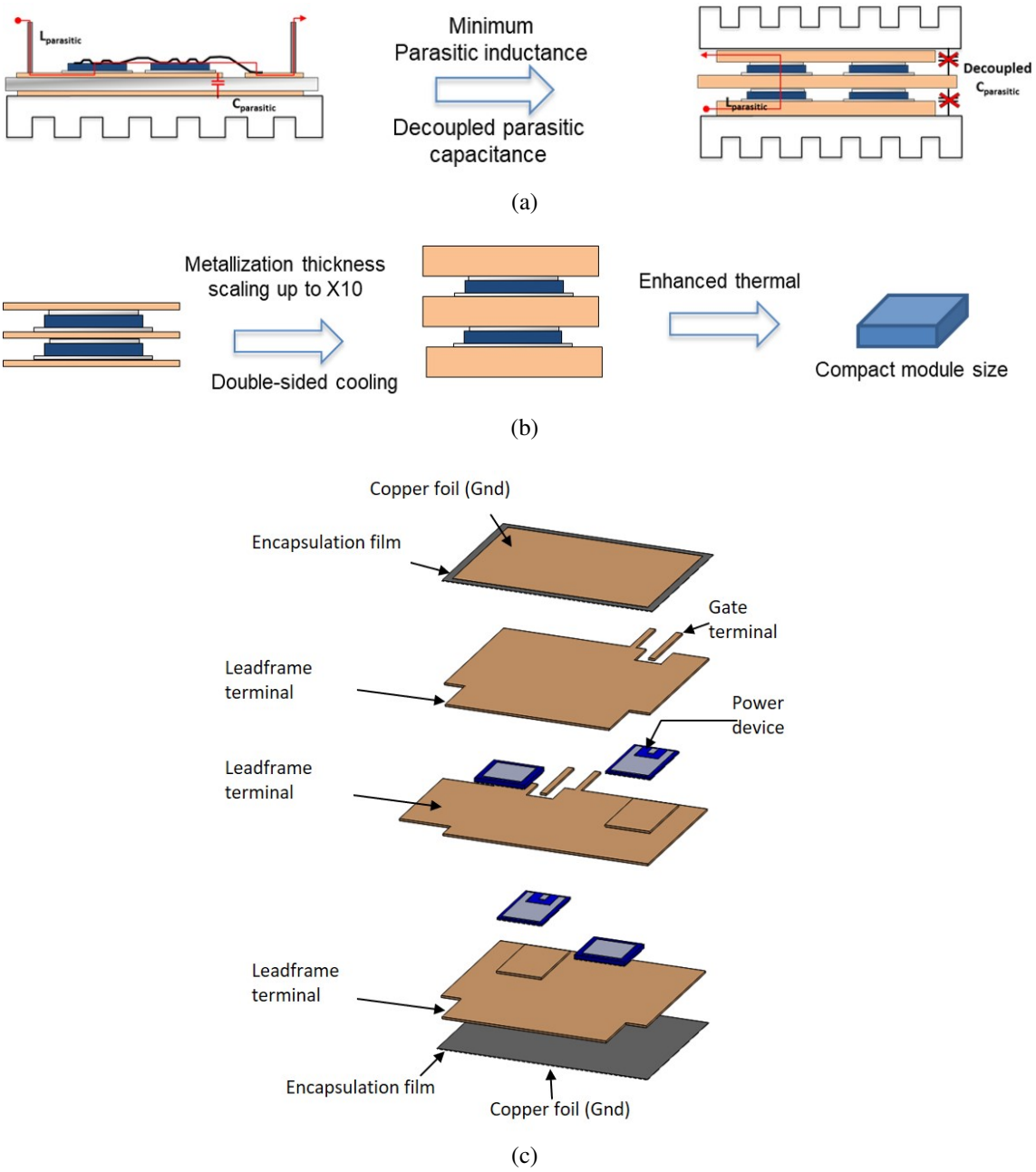


Figure 2.7: Georgia Tech Package Research Center's unique technical approach. (a) minimized parasitic using 3D structure for high-speed switching, (b) leadframe based heat spreading and double-sided cooling for enhanced thermal management.

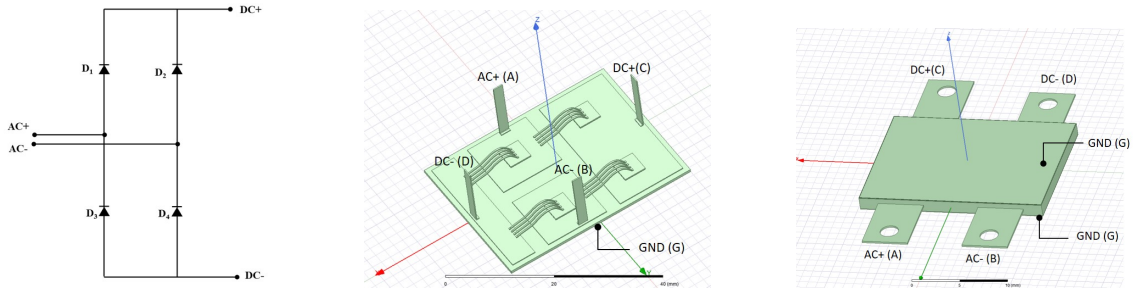
CHAPTER 3

DESIGN AND DEMONSTRATION OF 3D FULL BRIDGE RECTIFIER MODULE

The focus of this study was to design and demonstrate a 3D power module package with reduced parasitics and thermal resistance. A full bridge rectifier (FBR) configuration was selected as a first test-vehicle implementation to showcase the benefits of the proposed 3D power packaging technologies in achieving superior electrical and thermal characteristics, benchmarked against the conventional packaging approach. The manufacturing route, including defining the process flow, bills of materials and developing unit processes, was established, and the measurement results using active diodes are finally presented.

3.1 Moldeling of 3D FBR power module

Fig. 3.1(a) shows a circuit schematic that represents the FBR, and Fig. 3.1(b), (c) show two different designs of a full-bridge rectifier module. The conventional approach consists of four diodes assembled on the same X-Y plane, which is the Cu-metalized top surface of a



(a) (b) (c)

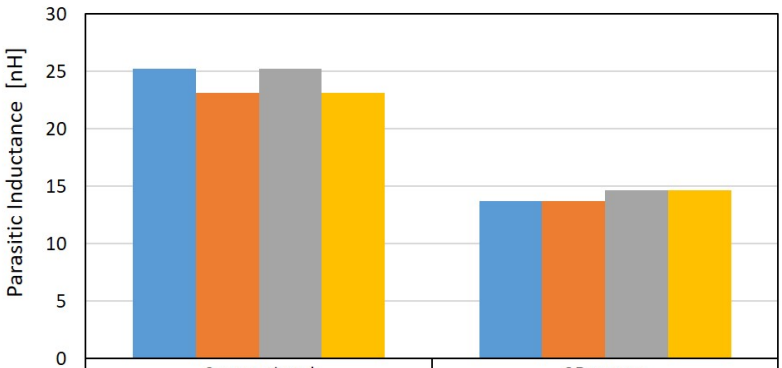
Figure 3.1: Modeling of full bridge diode rectifier. (a) Circuit schematic, (b) conventional power module, (c)3D power module.

DBC substrate, and the top side of the diodes are connected through wire bonds. On the other hand, the 3D power approach involves a pair of diodes stacked on top of each other to form a current path in the X-Z plane.

The preferred parasitics configurations for this type of module packages are suggested in [15]. Firstly, the inductances from terminal A to C (L_{AC}) and from terminal D to B (L_{DB}) should be as low as possible. Similarly, the inductances from terminal D to A (L_{DA}) and from terminal B to C (L_{BC}) should also be as low as possible. Thirdly, the parasitic capacitances between terminal A and ground (C_{AG}), and between terminal B and ground (C_{BG}) should be as small as possible. Symmetry between these two capacitances has a major effect on CM noise generation. Lastly, the parasitic capacitances between terminal C and ground (C_{CG}), and between terminal D and ground (C_{DG}) should be as large as possible. Large values of these parastics can help filter out common mode (CM) noise, and symmetry has minor impact on CM noise generation since the voltage fluctuation is relatively stable at these nodes.

The preferred parasitics configuration can be used as a criterion for designing the FBR power module. Considering these design guidelines, the parasitic inductances and capacitances were simulated for both packaging approaches using ANSYS Q3D, and compared. Fig. 3.2 shows the simulated parasitic inductances of the package. The extracted inductances between different terminals (L_{AC}, L_{DB}, L_{DA}, and L_{BC}) show that the 3D approach has on average a 40% reduction in the inductance values.

The parasitic capacitances of the DBC module depend heavily on the substrate geometry and choice of ceramic material used as substrate base. Assuming the ceramic material is fixed, the overlap- ping area between the conductor traces used as terminal nodes and



	Conventional	3D power
LAC	25.2	13.71
LDB	23.14	13.72
LBC	25.2	14.66
LDA	23.1	14.63

Figure 3.2: Comparison of extracted parasitic inductances

the bottom-side ground plane determines the parasitic capacitance values of the conventional package. On the other hand, the geometry and material stack-up for the 3D module is quite different from that of the conventional approach. Therefore, parametric studies on the isolation layers were carried out to identify which parameters dominate in the parasitic capacitance of such a 3D module.

Fig. 3.3(a) shows a simplified cross-section image of the FBR module defining the key parasitic capacitances. Fig 3.3(b),(c) shows the simulated parasitic capacitances considering varying thickness in a 50-300um range and dielectric constant in a 2-7 range of the thin-film isolation material. As previously mentioned, the critical parasitic capacitances for the CM noise generation are C_{AG} and C_{BG}. The simulation results show that the changes in dielectric constant or film thickness have little impact on those critical capacitance values, but do affect C_{CG} and C_{DG}. Based on the design preferences, an encapsulant film material with a dielectric constant of 6.8 and a film thickness of 50um was selected as an isolation layer. The resulting parasitic capacitance values of the 3D module are compared with that

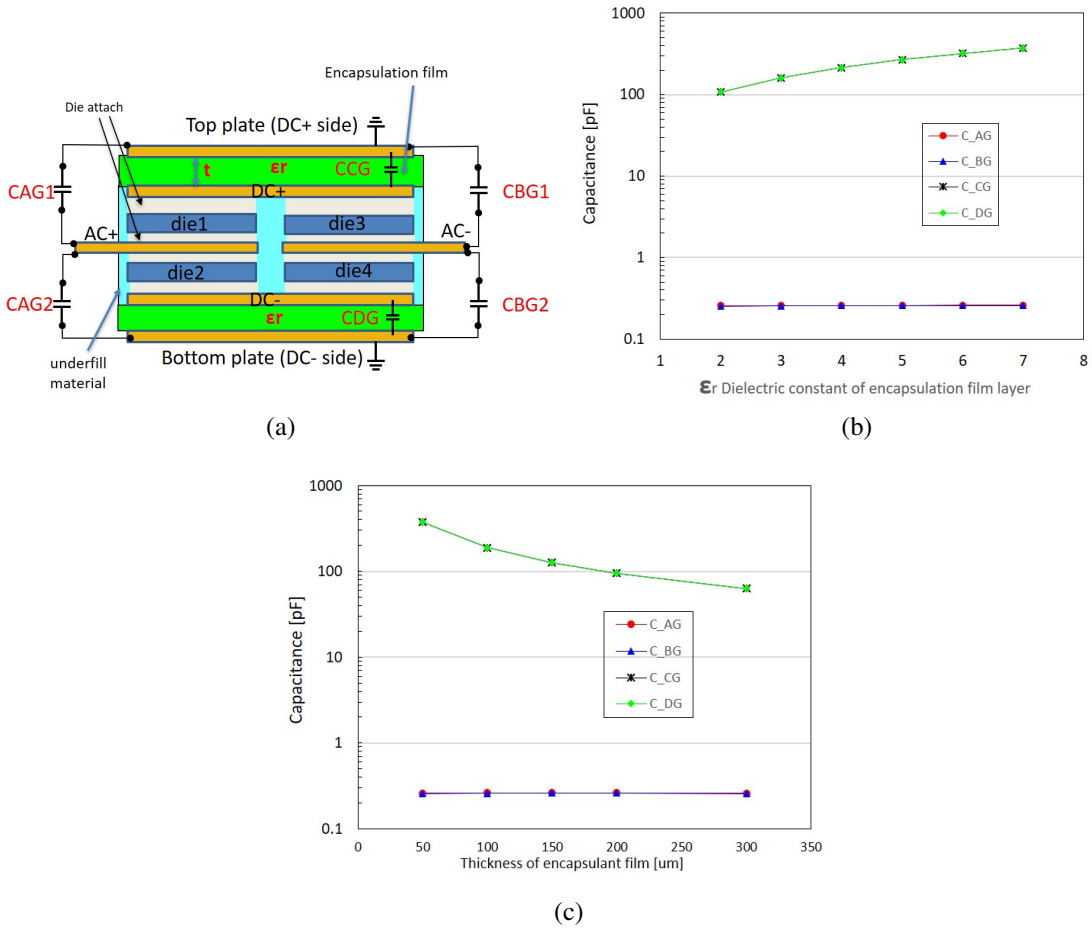


Figure 3.3: Modeling of 3D FBR with parasitic capacitances. (a) Cross-section of 3D FBR with parasitic capacitances, (b)capacitances with different dielectric constant when film thickness is 50um, (c)capacitances with different film thickness when dielectric constant 7.0

of the conventional DBC module in 3.4. This plot shows all capacitance values in the 3D approach are more desirable than in the conventional approach.

A finite element thermal model of the 3D stacked power package was built and run using ANSYS Workbench to evaluate its thermal dissipation performance, and see how the thickness of the isolation film, first optimized for the parasitic capacitances, affects the overall thermal behavior of the package. The internal heat generation from the die was assumed to be 100W per die, implemented as a volumetric heat source, and applied to a sin-

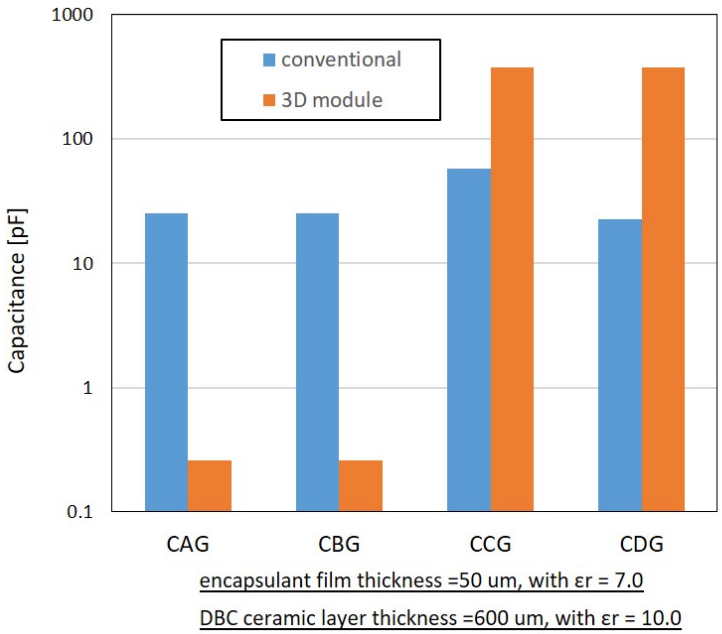


Figure 3.4: Comparison of extracted parasitic capacitances

gle diode. For the conventional module, as it is assumed that most of the heat is dissipated through the substrate and heat spreader, a heat transfer coefficient of 10,000W/m^{2}K was given only to the bottom-side of the heat spreader. On the other hand, for the 3D stacked module, the same value of heat transfer coefficient was given to both top and bottom side of the module assembly, as the structure allows for double-sided cooling. The thickness of the lead-frame was kept the same as the top-side copper trace of DBC, which is 200μm, considering sufficient current carrying capability and heat spreading effect.

Fig. 3.5 shows the junction-to-case thermal resistance simulation results for 3D stacked module, varying the thickness (from 50μm to 300μm) and thermal conductivity of the encapsulant film (from 0.15W/mK to 5W/mK). The thermal conductivity was found to have moderate impact on the overall thermal resistance of the package. The more thickness increases, the more conductivity matters. However, as long as the thickness of the film is maintained to a relatively low value (e.g. 50μm), the impact of the thermal conductivity

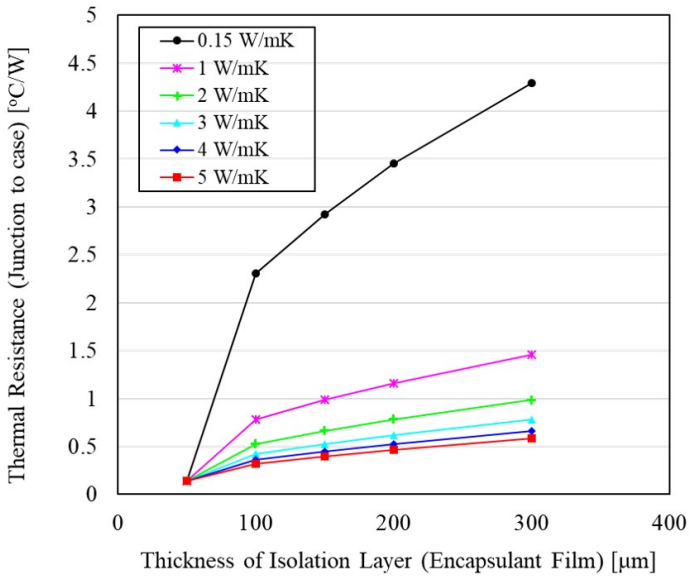
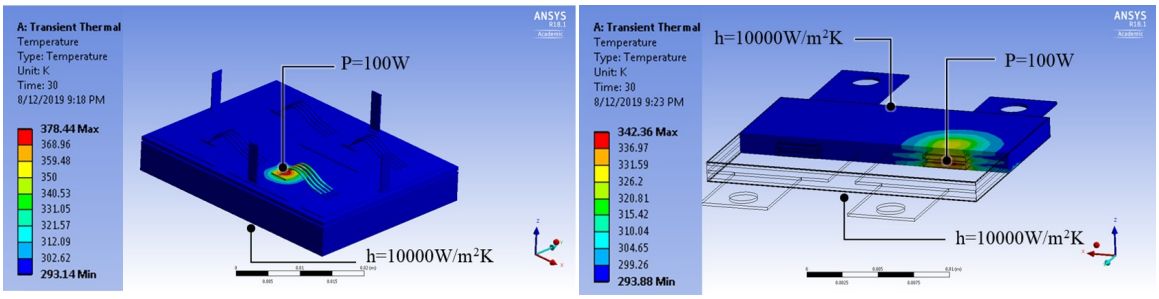


Figure 3.5: Simulation results for junction temperature rise.

is minimized. It is desirable to keep the thickness of the film as small as possible with adequate thermal conductivity (e.g. 2 - 5 W/mK) so long as the isolation requirements are satisfied. Encapsulant films with thermal conductivities greater than 5W/mK would typically require high filler contents with large filler sizes exceeding 60μm, limiting the thickness of the film that can be used as an isolation layer. Thus, when selecting the material for the isolation layer, it is critical to consider not only the thermal conductivity, but also the achievable thickness of the film.

A comparison of the simulation results of the resulting junction temperature rise in the two approaches is shown in Fig. 3.6. For the conventional approach, a typical Al_2O_3 ceramic layer with thermal conductivity of 24 W/mK and thickness of 600 μm, is assumed for the DBC substrate. Between the DBC substrate and the 5mm copper baseplate heat spreader, there is a solder substrate attach layer with a thermal conductivity of 58 W/mK. For the 3D module, the encapsulant film layers are assumed to be 65μm with a thermal

conductivity of 3 W/mK, and the sintered die-attach layers 45μm with a thermal conductivity of 240 W/mK. The material properties of different layers and their thicknesses are summarized in Table. 3.1. Owing to the double-sided cooling capability, advanced double-sided die-attach, and reduced number of package layers, the 3D approach shows about twice smaller thermal resistance, as summarized in Table 3.2.



(a) (b)

Figure 3.6: Simulation results of junction temperature rise when 100W is applied to the die with heat transfer coefficient of 10kW/m^{2}K applied to cooling interfaces. (a) Conventional module with heat spreader on the bottom of the DBC substrate. (b) 3D module with isolation layer thickness of 65μmm and thermal conductivity of 3 W/m·K.

Table 3.1: Layer thicknesses and material properties used in thermal simulations

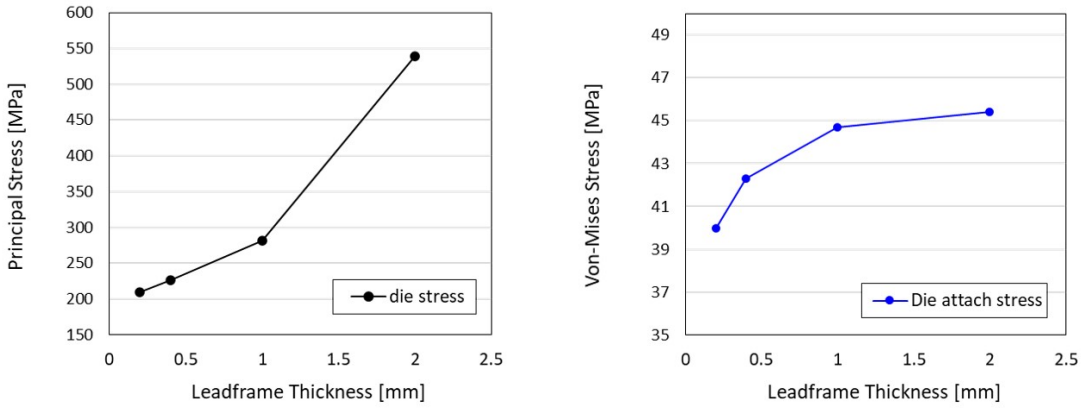
Layer	Material	Thickness	Thermal conductivity
DBC(Ceramic)	Al_2O_3	600 μm	24 W/mK
DBC(Copper)	Cu	300 μm	400 W/mK
Base plate	Cu	5 mm	400 W/mK
Die & substrate attach	Solder	50 μm	58 W/mK
Encapsulant film	Epoxy	65 μm	3 W/mK
Sintered die-attach	Ag	45 μm	240 W/mK
Leadframe	Cu	200 μm	400 W/mK

Table 3.2: Comparison of junction to case thermal resistance

	DBC Module	3D Module
Thermal Resistance (Junction-to-Case) [^{o}C/W]	0.83	0.38

The leadframe structures on both sides of the die with large area joints are desirable in terms of heat spreading effects, however, creates concern on the stresses that die attach layers and die experiences. In order to understand the impact of these leadframes on the stress on die and die attach, and plastic strain on the die attach, thermomechanical simulations were conducted with ANSYS Workbench. The goal was to calculate the stress on the die, and see if the stress level does not exceed the elastic limit of SiC dies, which is estimated to be around 1 GPa [96]. Moreover, the obtained stress and strain values of the die and die attach was compared with conventional packaging approach, to see the difference in the simulated values. Using the symmetry of the designed module, a quarter of the designed module was used in thermal stress simulations, saving necessary computational resources. A uniform temperature of 105^{o}C was applied to the entire model as a thermal load, and induced stress and strain on die and die attach were monitored as leadframe thickness was increased from 0.2mm to 2mm. The Anand visco-plastic model and bilinear kinematic hardening model were used for Ag sintered die attach and leadframe copper, respectively [97].

The simulation results of maximum stress and strain values are presented in Fig. 3.7. There was a significant increase in stress (equivalent principal) on the die as the leadframe thickness was increased from 0.2mm to 2mm. However, the principal stress values in all range of thicknesses were much below 1 GPa, which was the estimated limit for the acceptable value.The von-Mises stress on Ag sintered die attach showed a moderate increase from 40 MPa to 45 MPa (+12%), as the thickness of leadframe was increased. The equivalent plastic strain on Ag sintered die attach almost doubled from 2% to 4% as the leadframe thickness was increased from 0.2mm to 2mm. In order to understand how 3D module



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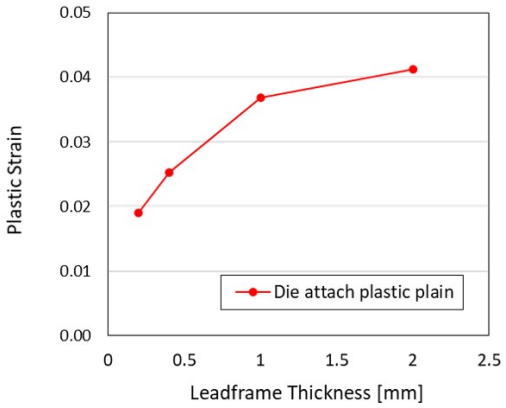
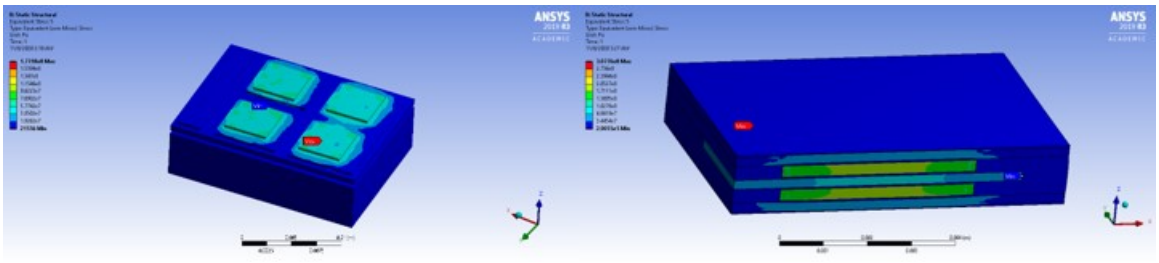


(c)

Figure 3.7: Thermomechanical simulation results. (a) Maximum principal stress on die, (b) maximum Equivalent (Von-Mises) stress on die attach (c) maximum plastic strain on die attach

would behave thermomechanically in comparison to the conventional module, the geometries in Fig. 3.6 were given the uniform thermal load as previously described. The summary of comparison is shown in Table. 3.3, and example plots of von-Mises stress on each structures are shown in Fig. 3.8. On the die side, the 3D module would experience higher stress, but both conventional and 3D approaches would result in die stress values that are much lower than the suggested limit of 1 GPa. On the die attach layers, 3D module showed 7% reduction in maximum von-Mises stress and 28% reduction in plastic strain. In conclusion,

under a uniform temperature elevation condition, 3D module would perform better on the die attach reliability, while the conventional would experience lower stress on the die. As long as the stress on the die does not exceed the elastic limit (or other indication of fracture limit), and is maintained sufficiently lower than the limit, 3D module structures are expected to perform better in terms of mechanical reliability under elevated temperatures.



(a) (b)

Figure 3.8: Thermomechanical simulation results. (a) Equivalent (Von-Mises) stress on conventional module, (b) Equivalent (Von-Mises) stress on 3D module.

Table 3.3: Comparison of stress and strain values for conventional and 3D modules at uniform elevated temperature of 105°C

	Parameter	Conventional module 5mm	3D module 0.2mm
Die	Maximum Principal Stress [MPa]	174	233 (+34%)
Die Attach	Maximum Von-Mises Stress [MPa]	43	40 (-7.0%)
Die Attach	Maximum Plastic Strain	2.69e-2	1.90e-2 (-28.3%)

3.2 Fabrication of 3D FBR Power Module

As the proposed 3D power module is based on a leadframe substrate instead of DBC, the fabrication of the module starts with preparing patterned copper(Cu) lead-frames. A Cu plate with a thickness of 210 μm was patterned using a wet etching process, and surface finished with Nickel/gold (Ni/Au) to promote adhesion of the die-attach layers. The overall assembly process flow for stacking of the power dies is shown in Fig. 3.9. A commercial

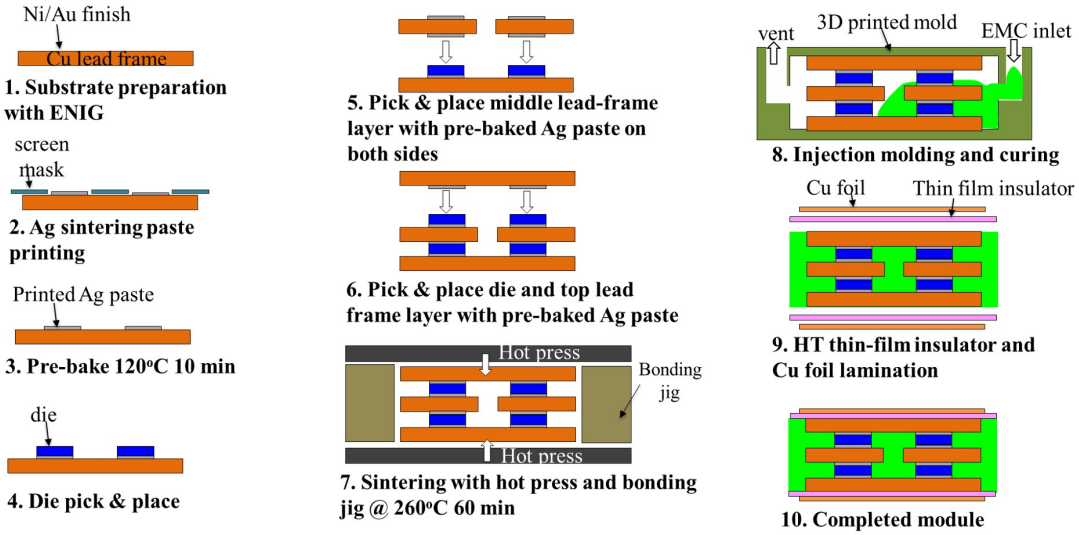


Figure 3.9: Assembly process flow for 3D power module test-vehicle

Table 3.4: Materials and components used in the test-vehicle

Item	Description
Die-attach	Ag sintering paste from Heraeus (ASP-016)
Mold compound	Capillary underfill from Namics
Encapsulant film	Epoxy-based encapsulant sheet from Nagase
Lead-frame	Wet-etched 210 μm Copper with Ni/Au finish
Die	200V/15A Silicon diode from SMC with Ag finish

silver (Ag) sintering material, ASP-016 from Heraeus, was used to attach the dies. The Ag paste material was applied on the finished surfaces of the lead-frames, and baked at 120°C to dry the solvent content within the paste. Then, the dies and Ag-printed lead-frames were placed in a bonding jig for the sintering process to build the 3D stack in a single processing step. The bonding jig served as a means to align the components as well as to control the bondline thickness of the sintered Ag joints. The sintering process was done using a hot press from PHI hydraulics applying 12MPa at 260°C for 60 minutes. After sintering, the

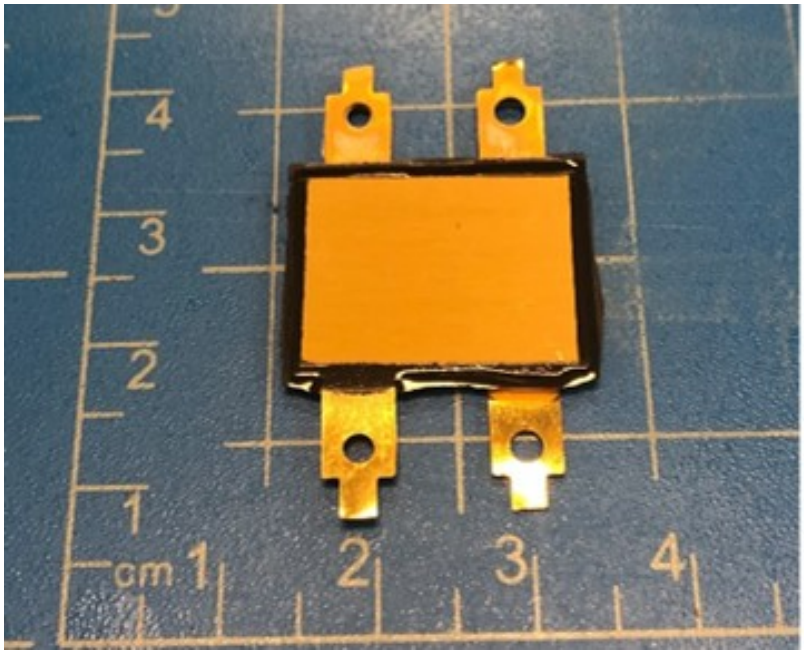
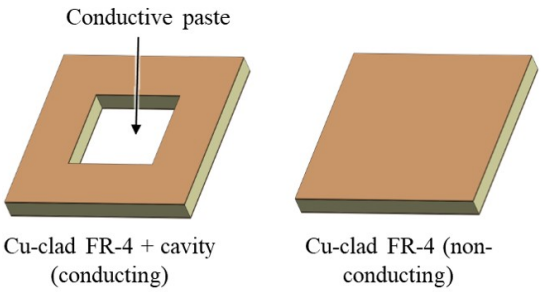


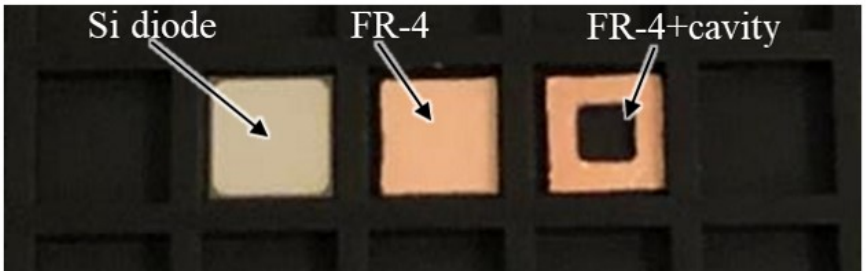
Figure 3.10: The 3D stacked power module test-vehicle after completion of the assembly processes

gaps between the Cu plate terminals were filled with a commercial underfill material to emulate injection molding. Lastly, the outer surface of the lead-frames (DC terminals) are isolated from the Cu foil layers (ground terminals) with high thermal conductivity encapsulant films using a Meiki vacuum laminator. The description of materials and devices used for this test-vehicle implementation is detailed in Table. 3.4. The completed module has a size of 20 mm$\times$15mm$\times$1.5 mm (W $\times$ L $\times$ H) as shown in Fig 3.10.

The parasitic elements of the silicon diodes make it difficult to measure the parasitics solely resulting from the package. Therefore, two additional test vehicles were built, as shown in Fig. 3.11, using a similar process flow for ease of measurement of the package parasitic inductances and capacitances. The first one involves a conducting dummy die that replaces the diode for measurement of the parasitic inductances. This first dummy die is made of a Copper-clad FR-4 block, diced into the size of the diode, with a through-



(a)



(b)

Figure 3.11: Dummy test vehicles for parasitics measurements. (a) Images of designed dummy dies for conducting and non-conducting measurements, (b) images of active diode die and fabricated dummy dies.

hole cavity filled with a conductive paste to form an electrical connection between the lead-frames. The second test vehicle included a non-conducting dummy die for parasitic capacitance measurements between the terminals. The second dummy die is essentially the same FR-4 block attached using the same conductive paste, but without the cavity, isolating the lead-frames.

The completed module with silicon diodes is cross-sectioned and polished to verify the suitability of the developed assembly process, as shown in Fig. 3.12. Each layer is individually labeled in the overall module view of Fig. 3.12(a). The magnified image of the stacked diodes in Fig. 3.12b) shows uniform bondline thicknesses of all die-attach layers with no observable cracking on the diodes, indicating the pressure control using the bonding jigs was indeed successful. Suitable adhesion of die-attach layers was also confirmed

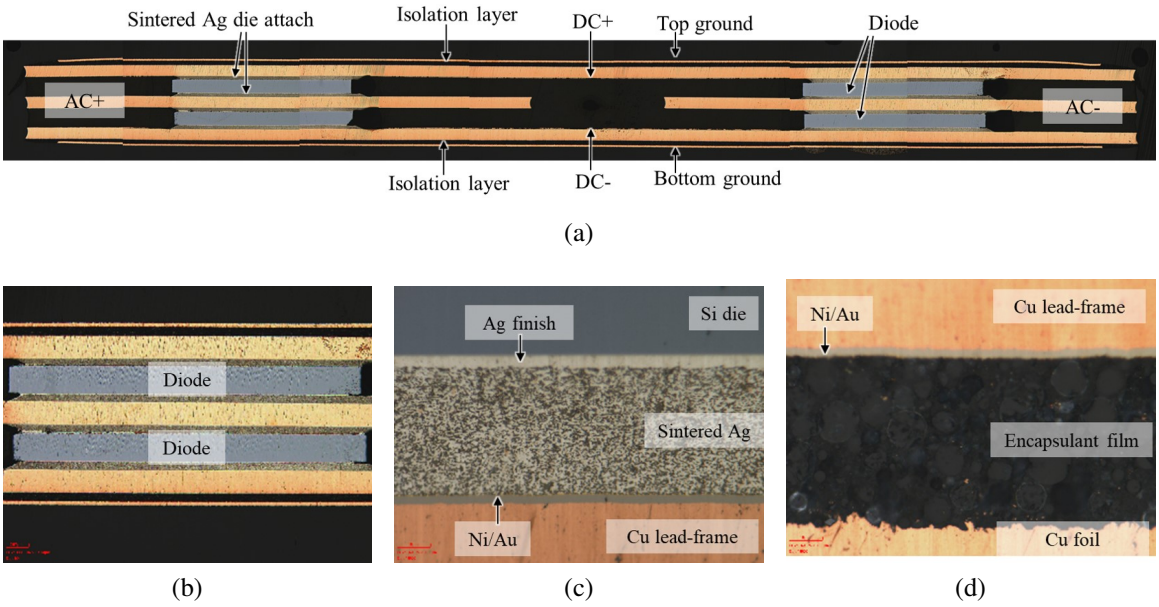
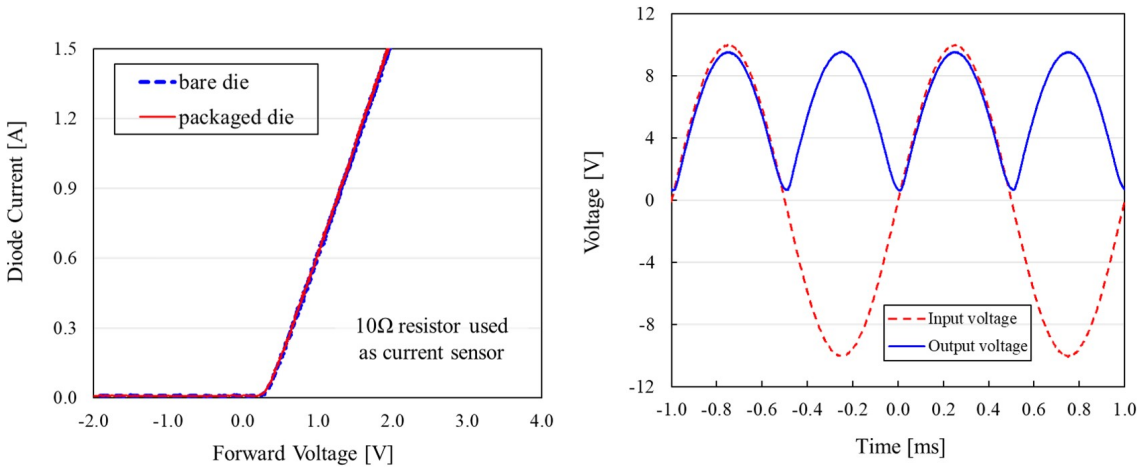


Figure 3.12: Optical microscope images of the module cross-section. (a) Stitched images of overall module, (b) magnified image of stacked diodes, (c) sintered Ag die-attach layer (c) laminated encapsulant film

with no delamination or void present at the bonded interfaces, confirming that the die and lead-frame surface metallizations (i.e. Ni/Au surface finish) are, as expected, compatible with the Ag sintering process. On the inspected cross-section area, the encapsulation film layers also show good adhesion to both Cu interfaces with no delamination or voids. These results indicate that the proposed 3D stacking process using a simple single-step sintering process is a viable industry-compatible solution for manufacturing of such complex 3D architecture.

3.3 Characterization of the 3D Power Module

The I-V curve of the diode and input/output waveforms of the module were measured using Keysight function gen- erator (33500B) and Keysight oscilloscope (DSOX4054A), to evaluate functionality of the fabricated 3D module. The characteristic I-V curves of the diode



(a) (b)

Figure 3.13: Measurement of 3D stacked module. (a) I-V curve of a diode before and after the packaging process, (b) input and output waveforms of full-bridge rectifier with a resistive load

before and after the 3D assembly process were measured, as shown in Fig. 3.13(a). When measuring the bare die, wires were attached to both top and bottom of the die using silver epoxy for easier connection to the probes. For both bare and packaged dies, a 10 Ω resistor was used as current sensor. The measured I-V curves before and after packaging show almost identical characteristics, indicating that the fabrication process and the packaging itself have no significant impact on the diode's static characteristics. The input and output waveforms of the rectifier were also measured. A sine wave input of 10V peak voltage was provided from the function generator to the 3D FBR module with a simple resistor load of 78 kΩ, as shown in Fig. 3.13(b). The plot shows the rectified output with a 0.43 V drop in the peak voltage from the diodes. This indicates that all four diodes in the module are packaged correctly without any open or short defects on the interconnections.

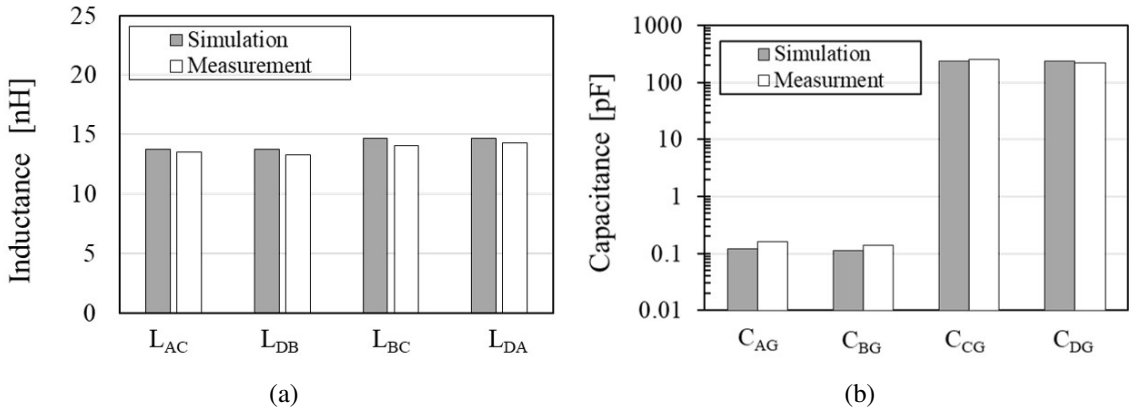


Figure 3.14: Parasitics measurements of the fabricated 3D stacked module: (a) parasitic inductances between different terminals; and (b) parasitic capacitances between different terminals

3.3.1 Parasitics measurements

The parasitic inductances and capacitances of the 3D stacked power module package were finally measured using the test vehicles with conducting and non-conducting dummy dies. The parasitics' values between the different terminals were measured with a HP 4285A precision LCR meter (75kHz - 30MHz), and are summarized in Fig. 3.14.

The measured inductance values ranged from 13nH to 14nH, including the length of the terminals, with less than 4% difference between measurements and simulations. On the other hand, the capacitance values were measured for the the four terminals (A, B, C, and D) with respect to ground terminals. These inductance measurements confirm that the 3D stacking approach could result in much smaller inductances compared to the inductance values of the conventional module simulated in Section II-A, which had values ranging from 23nH to 25nH. The average capacitance of the AC terminals (C_{AG} and C_{BG}) were measured at 0.15pF which was about 30% higher than the simulated values. This deviation may be attributed to approximations in material properties used in the simulations, as

well as the presence of fringe fields between the terminals. The capacitance values of the DC terminals (C_{CG} and C_{DG}) were measured to be 238 pF on average, with less than 9% difference with the simulation. The capacitance measurements confirm around 100 times reduction in C_{AG} and C_{BG}, and around 4 times increase in C_{CG} and C_{DG} compared to the simulated values of conventional module, which indicates the 3D stacking approach provides desirable package parasitic capacitances that would minimized the CM noise. These results show that the simulated values in the modeling section are in good accordance with the parasitics inductance and capacitance values of the fabricated power module package.

3.3.2 Thermal resistance measurement

$$K = |\frac{T_{high} - T_{low}}{V_{high} - V_{low}}| \qquad [^oC/V] \tag{3.1}$$

The thermal resistance of the 3D FBR was also measured to verify the thermal modeling predictions. As attaching a thermocouple on the case where the hot spot is might distort accurate measurements, and as it was difficult to implement a thermocouple in between the case and heat spreader, junction-to-ambient thermal resistance was measured and simulated again with boundary conditions closer to the actual measurement set-up. While a simple thermometer can be used to monitor the ambient temperature, an indirect measurement method is used to assess the junction temperature as the diodes were embedded inside the module which did not allow direct access to measure the junction temperatures. The change in junction temperature of a diode result in change in junction forward voltage with a constant correlation factor K as expressed in Eq. 3.1, where T_{low} and V_{low} are initial measurements at stabilized room temperature, and T_{high} and V_{high} are measurements taken

at elevated temperatures [98]. Using the temperature-dependence of the forward voltage drop of the diode, the relationship between a diode's forward voltage and its junction temperature was characterized using a convection oven to extract the coefficient K as shown in Fig. 3.15. Using this K value, the junction temperature rise could be derived by monitoring the change in the forward voltage drop in the module as shown in Fig. 3.16(a), with a Keithley 2400 used as a source meter. An additional thermal simulation was carried out with the same materials and package design modeled in section II-B, but with different environmental conditions to more closely emulate the junction temperature rise measurement set-up, as shown in Fig. 3.16(b). All outer surfaces in the model were set to have a heat transfer coefficient of 20 W/m^{2}K with an ambient temperature of 19.6^{o}C, and the diode was input with 0.95W, which corresponds to the value applied in the actual measurements. The simulated and experimental junction-to-ambient thermal resistance values are reported in Table. 3.5, and are in great accordance with modeling results, with only about 2.5% deviation. These results indicate that thermal modeling represented the thermal performance of the 3D FBR module package very accurately. From this thermal characterization, and from the results of thermal modeling in Section II-B, it can be inferred that the 3D stacking approach can achieve low-thermal resistance package by eliminating package layers and removing wire bonds which allow double-sided cooling of the module.

Table 3.5: Comparison of junction-to-ambient thermal resistance

	Simulation	Measurement
Thermal Resistance (Junction-to-Ambient) [^{o}C/W]	20.0	19.5

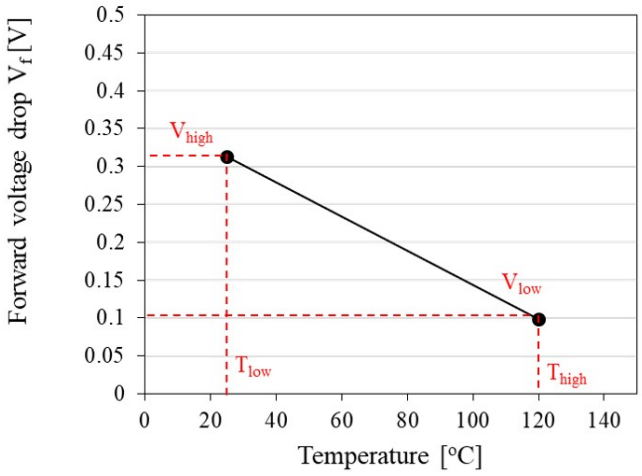
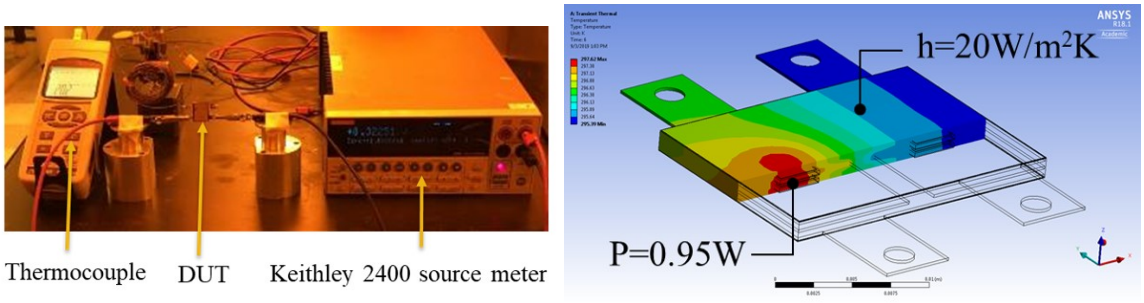


Figure 3.15: Thermal characterization of a diode within the FBR. The K factor was calculated using the slope measured in the plot.



(a) (b)

Figure 3.16: Junction-to-ambient thermal resistance measurement and simulation. (a) Measurement set-up for junction temperature rise. (b) simulation set-up for junction-to-ambient thermal resistance.

CHAPTER 4

DESIGN AND MODELING FOR 3D HALF-BRIDGE MODULE

4.1 Thermal modeling for half-bridge module

As an essential building block of power converters, half-bridge modules are one of the most widely used device configurations that are commercially available. In this chapter, a 3D stacked package design for half-bridge module is studied to achieve low-parasitics, and enhanced thermal performance than the conventional packaging approach. A half-bridge module package will be first thermally optimized for the layout size with a specification given in Table 4.1. Secondley, the electrical parasitics will be studied with different parametric designs to determine the impact of terminal designs to the extracted parasitics. For these design studies, a reference model for conventional module will be designed in parallel for comparison.

Table 4.1: Specifications for half-bridge power module

Specifications	Value
SiC MOSFET	1200V / 50A, R_{on}=10.5mΩ
SiC Diode	1200V / 50A
V_{DC}, I_{DC} of converter	800 V / 20 A
Coolant temperature	70^{o}C
Heat transfer coefficient of cooling technology	5000 W/m^{2}K
Maximum junction temperature	$\leq$ 150^{o}C
Heat flux per die	300 W/cm^2

The specifications for the power module is presented in Table 4.1. The target application was assumed to be motor drive power converters for electric vehicles when selecting these values. These parameters were used to determine the electrical and thermal boundaries

in the modeling studies. A baseline concept drawings for conventional and 3D stacking approaches are shown in Fig. 4.1 and Fig. 4.2, respectively. The conventional approach has DBC substrate where the power devices are attached onto it with solder die attach. The ceramic layer in the middle of DBC acts as isolation layer preventing the current to flow to the baseplate and cooling systems. The top-side of the power devices are connected with Al wirebonds to form electrical connections for gate signal and power. On the other hand, 3D stacked module is a leadframe-based package, where the power dies are attached onto top and bottom leadframes with sintered silver die attach. The electrical isolation to the cooling system is achieved with high-thermal conductivity encapsulant films on both top and bottom sides of the module. The gate terminals are directly patterned on leadframes, and the top, middle and bottom leadframes act as power terminals.

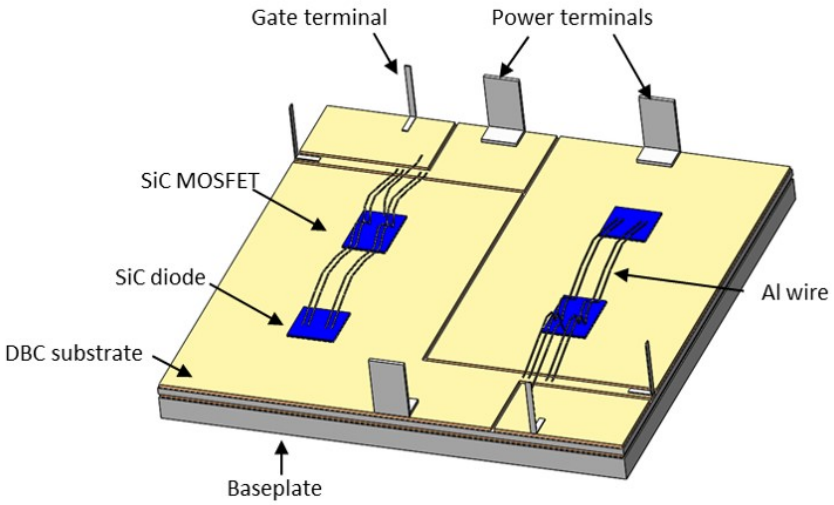


Figure 4.1: Package design for conventional half-bridge power module

In order to estimate the required footprint of the modules to satisfy the heat dissipation and cooling conditions given in Table. 4.1, baseline models were created for the two approaches (conventional, 3D stack). The smallest footprint that could physically accom-

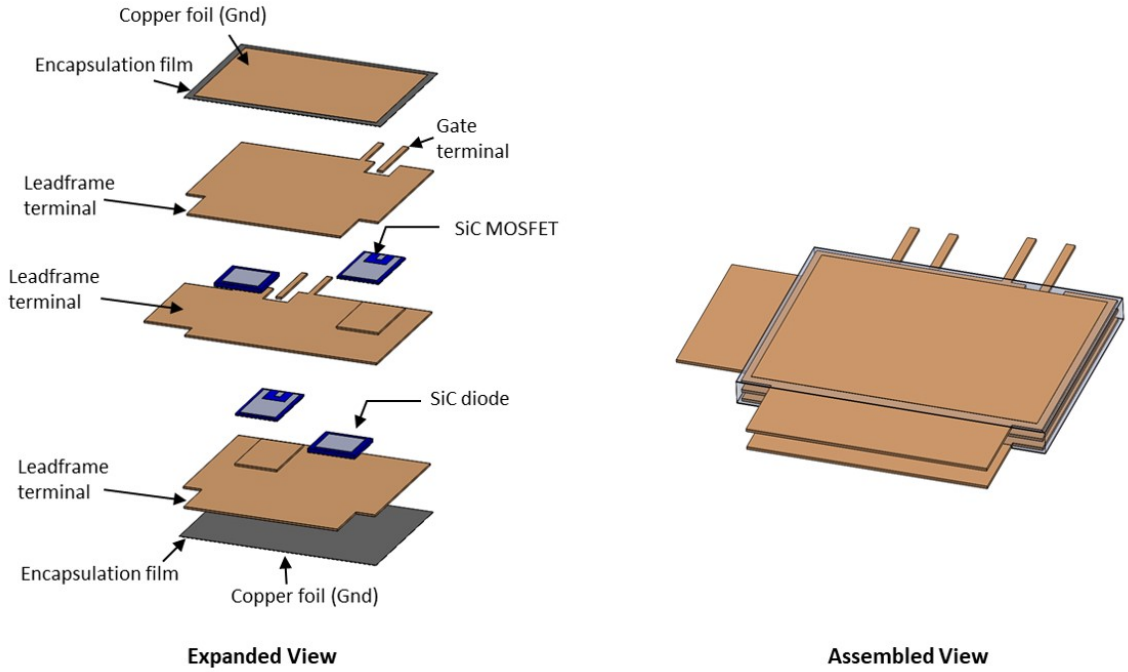


Figure 4.2: Package design for 3D stacked half-bridge power module

modate two MOSFETs and two diodes, for top and bottom switch positions, considering the separation gaps for isolation was selected as the baseline models. From these baseline models, the footprint sizes were increased incrementally as shown in Table. 4.2 to identify what size would be needed for the devices to reach junction temperatures below 150°C. Thermal simulation was conducted with these models with different footprint sizes using ANSYS Workbech to obtain maximum junction temperatures of devices. The simulation set-up for conventional and 3D stacked approaches are depicted in Fig. 4.3. The effects of terminals in both cases were neglected for simplicity in the simulation processes. In the conventional case, the heat flux of 300W/cm^2 is applied to all the MOSFET and a diode pairs (both top and bottom switch positions), and the bottom side of the module is defined as convention with heat transfer coefficient(HTC) of 5000W/m^{2}K at an ambient temperature of 70°C to represent a liquid cooling cold plate. Similarly, for the 3D stacked case, the

heat flux of 300W/cm^2 is applied to all the devices (both top and bottom switch positions), and the same convection is defined on both top and bottom surfaces of the module to represent double-sided liquid cooling. Although it barely affect the results, the remaining outer surfaces of the models were defined as natural air convection with HTC of 10W/m^{2}K at ambient of 22^{o}C for both cases.

Table 4.2: Module footprint size increments for thermal optimization

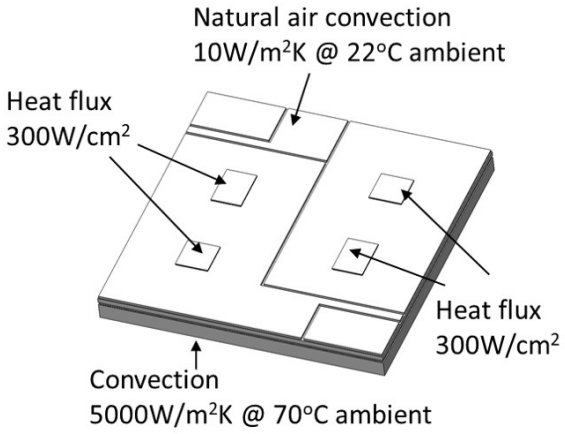
Conventional [mm^2]	**3D stacked [mm^2]**
15 × 20 (baseline)	15 × 20 (baseline)
20 × 20	20 × 20
25 × 20	25 × 20
30 × 25	30 × 25
30 × 30	30 × 30
35 × 35	35 × 35
40 × 40	40 × 40
50 × 50	50 × 50

Table 4.3: Layer thickness, materials, and their thermal conductivity properties for conventional module

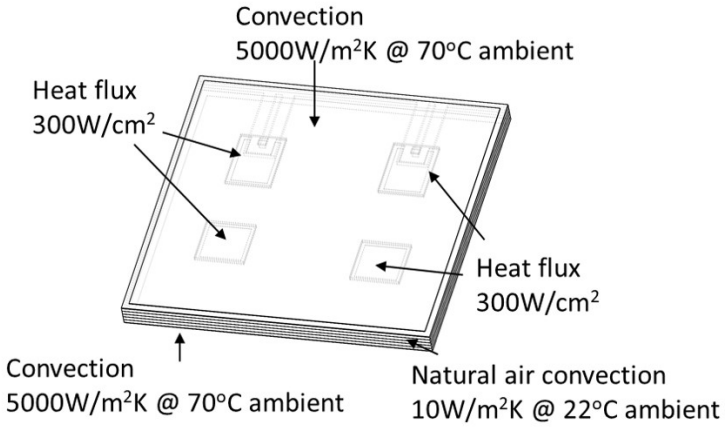
Layer	**Thickness [μm]**	**Material**	**Thermal conductivity [W/mK]**
Top metal	300	Copper	400
Ceramic	600	Al_2O_3	30
Bottom metal	300	Copper	400
Die (substrate) attach	50	SAC305	48
Diode	130	SiC	370
MOSFET	130	SiC	370
Baseplate	2000	Copper	400

Table 4.4: Layer thickness, materials, and their thermal conductivity properties for 3D stacked module

Layer	**Thickness [μm]**	**Material**	**Thermal conductivity [W/mK]**
Top leadframe	300	Copper	400
Middle leadframe	300	Copper	400
Bottom leadframe	300	Copper	400
Die attach	50	Ag sintered joint	240
Diode	130	SiC	370
MOSFET	130	SiC	370
Encapsulant film	50	epoxy	3
Copper foil	50	Copper	400
Stand-off spacer	100	Copper	400
Molding compound		epoxy	0.5

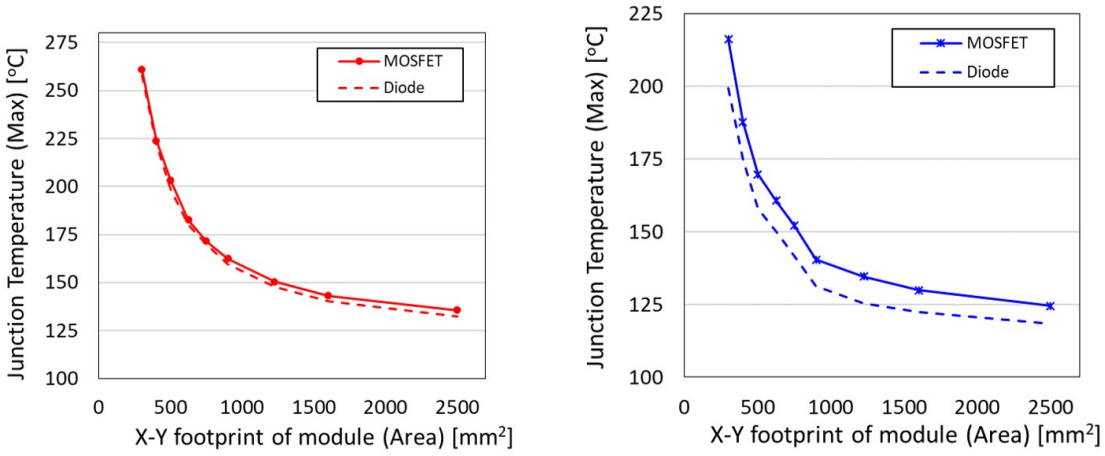


(a)



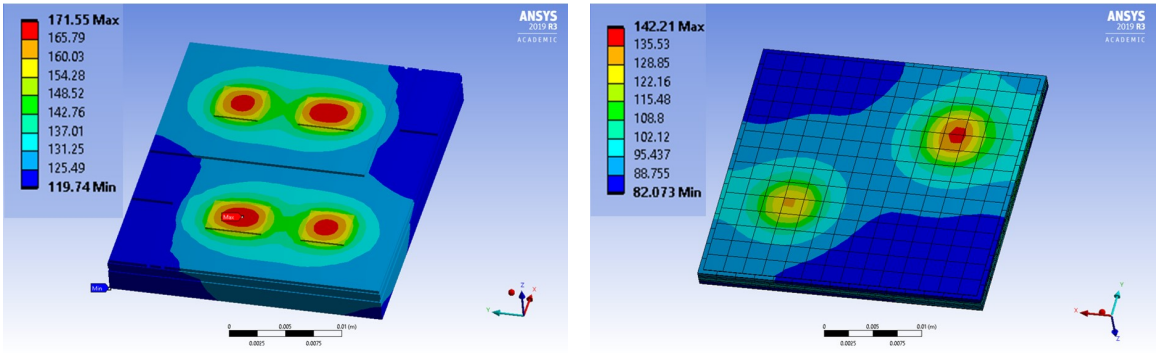
(b)

Figure 4.3: (a) simulation set-up for conventional module, (b) simulation set-up for 3D stacked module.



(a) (b)

Figure 4.4: (a) Junction temperatures for conventional module, (b) Junction temperatures for 3D stacked module.



(a) (b)

Figure 4.5: (a) Temperature distribution of overall conventional module at $30\times25mm^2$, (b) Temperature distribution of overall 3D stacked module at $30\times30mm^2$

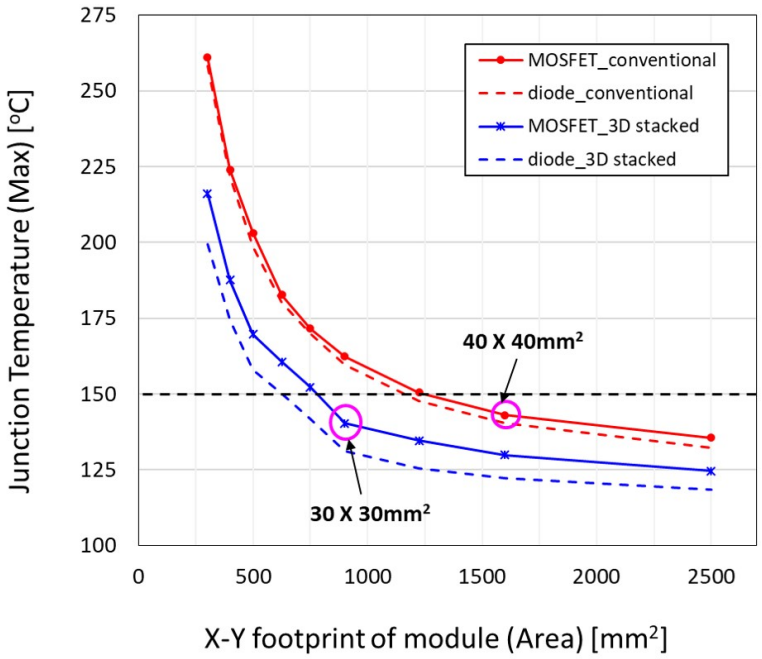


Figure 4.6: Comparison of maximum junction temperatures with increasing module footprint area. The horizontal dotted black line indicates maximum limit temperature, and pink circles indicate points with minimum footprint areas for each module approaches.

Table 4.5: Thermal resistance comparison for conventional and 3D stacked modules

Parameter	**Conventional module**	**3D stacked module**	**3D stacked module**
Area (Tj<150°C)	40 X 40 mm^2	30 X 30 mm^2	40 X 40 mm^2
Thermal resistance (Junction-to-coolant)	1.28°C/W	1.23 °C/W	1.05 °C/W

The results for the thermal simulations of conventional approach and 3D stacking approach are shown in Fig. 4.4(a) and and Fig. 4.4(b), respectively. Both curves in Fig. 4.4(a),(b) show decreasing junction temperature as the X-Y footprint of the modules are increased. As the footprint area gets larger, the junction-to-coolant thermal resistance reduces, which results in the decrease in junction temperatures of power dies. Moreover, in both cases, MOSFETs show slightly higher junction temperatures compared to the diodes. Thus, the

MOSFETs become the limiting factor when determining the minimum footprint of the module.

An example of temperature distribution plots of the two modules at different areas are shown in Fig. 4.5. The junction temperatures of both conventional and 3D stacking approach is compared in Fig. 4.6. The objective of this thermal simulation was to find the minimum module footprint that is below the black dotted line in Fig. 4.6,which indicates the maximum junction temperature (150^{o}C) of the dies. As indicated with pink circle in Fig. 4.6, the minimum area for conventional module was 40×40mm^2, while the minimum area for the 3D stacked module was 30×30mm^2.

In conclusion, given the same thermal boundary conditions, the 3D stacked module would require smaller module footprint area compared to the conventional modules. In other words, if the conventional and 3D stacked modules were to have the same footprint size, the thermal performance of the 3D stacked module would be better than the conventional module. The thermal performance can be understood in terms of thermal resistance (junction-to-coolant) as shown in Table. 4.5. The comparison in thermal Resistance values shows that the 3D stacked module has about 18% reduction in thermal resistance (junction-to-coolant) compared to the conventional module at the same module size of 40mm$\times$40mm.

4.2 Electrical modeling for half-bridge module

Based on the selected module size for 3D stacked approach, various terminal arrangements and 3D modules were modeled and simulated using ANSYS Q3D to find what design features impact the parasitic inductance (power loop inductance) of the 3D structure. The

power loop inductance is defined in each module as the inductance extracted form the positive terminal to the negative terminal. Firstly, the effect of terminal length is studied as presented in Fig. 4.7. As the length of P and N terminal gets longer, the inductance increases as the current path gets longer from P-to-N terminals.

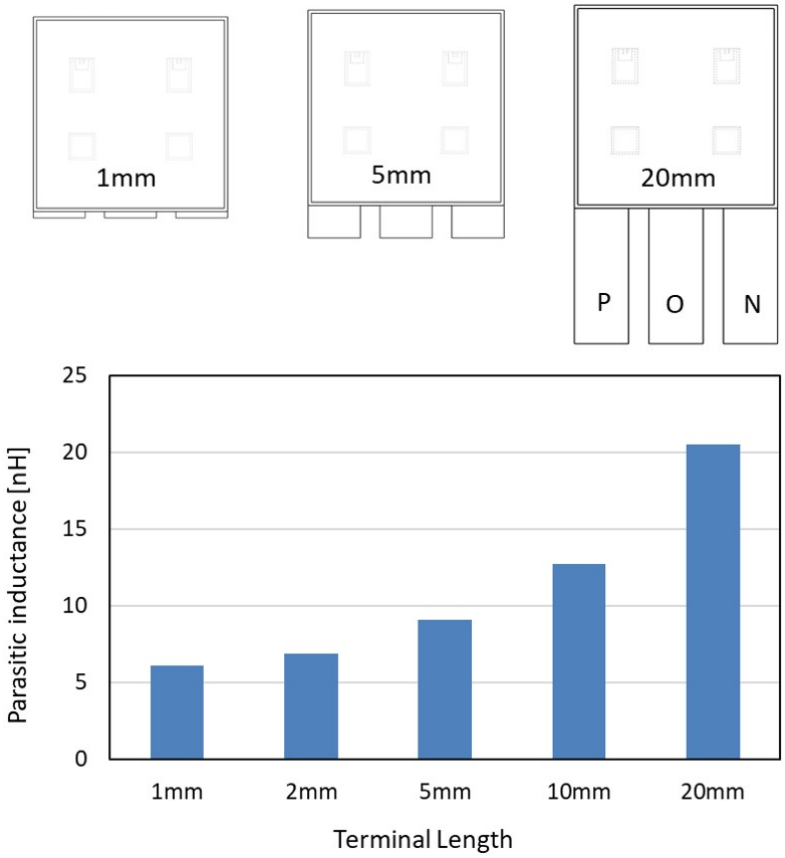


Figure 4.7: The impact of terminal lengths on parasitic inductance of the module.

Secondly, the impact of increasing the number of dies in the power loop inductance was studied. Assuming the current rating of the module need to be changed by adding or subtracting the number of dies per position, three different modules with 1 MOSFET and 1 diode per switch position(parallel 1), 2 MOSFETs and 2 diodes per switch position(parallel 2), and 3 MOSFETS and 3 diodes per switch position(parallel 3) are modeled as shown in Fig. 4.8. When increasing the number of paralleled devices, the area of the module was

increased proportionally to the number of paralleled devices (ex. 3×area of parallel 1=area of parallel 3). As the area of the module gets increased as more number of paralleled dies are assembled, it is inevitable to have increasing parasitic inductance when the module gets larger with the terminal arrangements are shown in Fig. 4.8. Thus, the increasing number of paralleled devices, or increasing the current rating of the module would result in increased parasitic inductance.

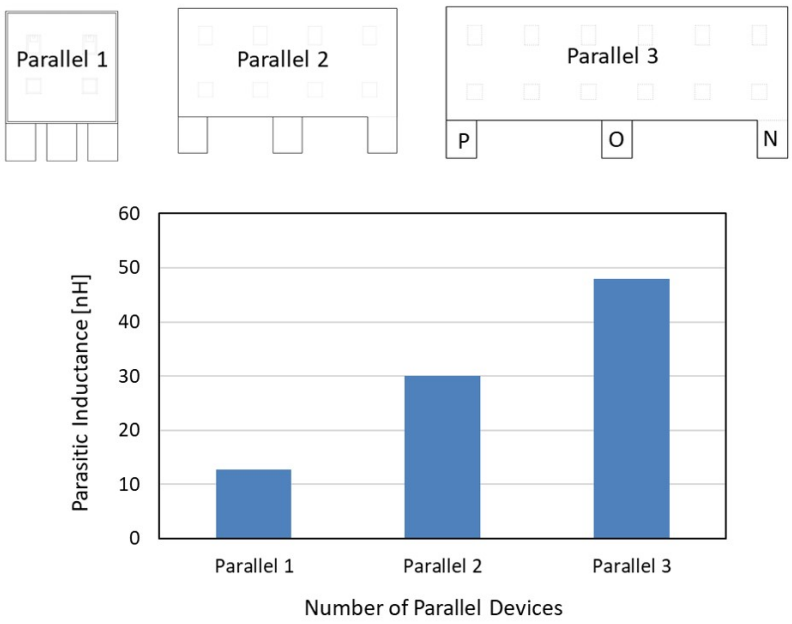


Figure 4.8: The impact of number of paralleling devices on parasitic inductance of the module.

Thirdly, the impact of overlap area between P-N terminal on parasitic inductance was studied. Different from previous terminal arrangements, where the P, O, and N terminals were positioned side-by-side, the output terminal in the middle were arranged on the side of the module, and the P-N terminal widths were gradually increased to create more overlapping area between them as depicted in Fig. 4.9. As the overlapping area between P-N terminals is increased, the parasitic inductance decreases significantly. The baseline mod-

ule with 0% overlap has inductance of 15nH, whereas the module with 100% overlap has inductance of 0.6nH. This drastic decrease in inductance is attributed to the magnetic field cancellation between these two terminals. The unique structure of 3D stacked module allows this P-N terminal overlap arrangement, which makes the same amount of current to flow in opposite directions to induce the magnetic field cancellation.

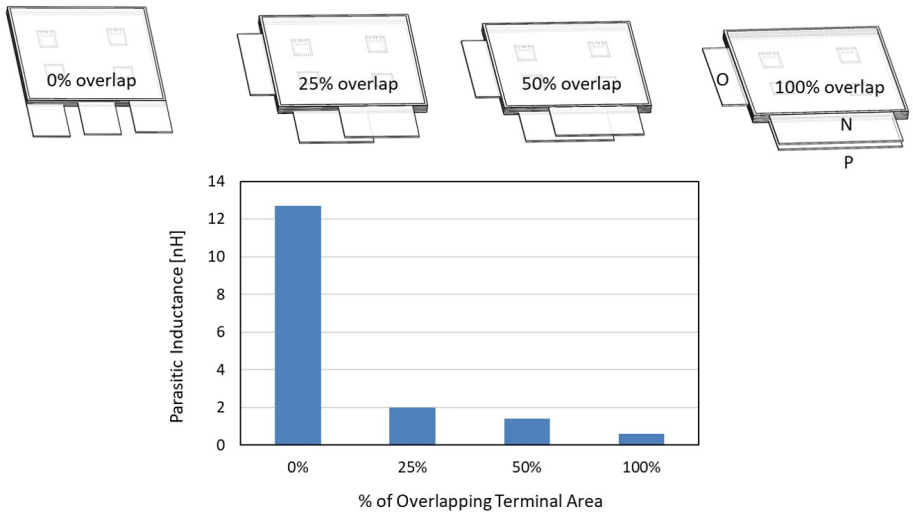


Figure 4.9: The impact of overlapping area between P-N terminals on parasitic inductance of the module.

Finally, based on previous studies, the impact of overlap area in combination with the number of paralleling devices were studied to find out if the overlapping terminal area would still reduce the parasitic inductance significantly in increased module sizes. The modules in Fig 4.10 are variations from the modules in Fig 4.8, which have increasing number of paralleling devices. The terminal arrangements for the modules with increasing number of devices were modified to have 100% area overlap between the P-N terminals, and the extracted parasitic inductance is shown as red triangle marker in Fig. 4.10. The results show that parasitic inductances of modules with increasing number of devices main-

tain significantly low parasitic inductance $\leq$0.6nH regardless of increased module footprint area. From these various parametric studies regarding power loop parasitic inductance of the 3D stacked modules, it can be concluded that the arrangement of terminals (P-N) becomes critical in reducing the parasitic inductance.

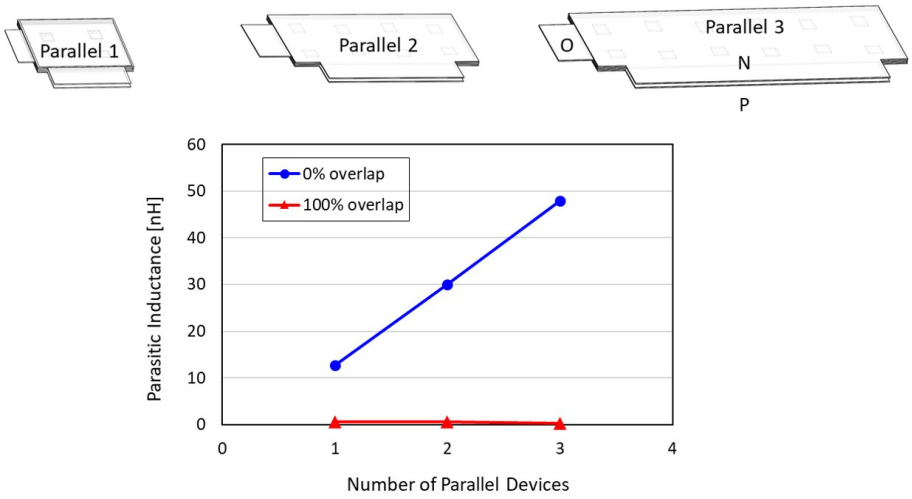
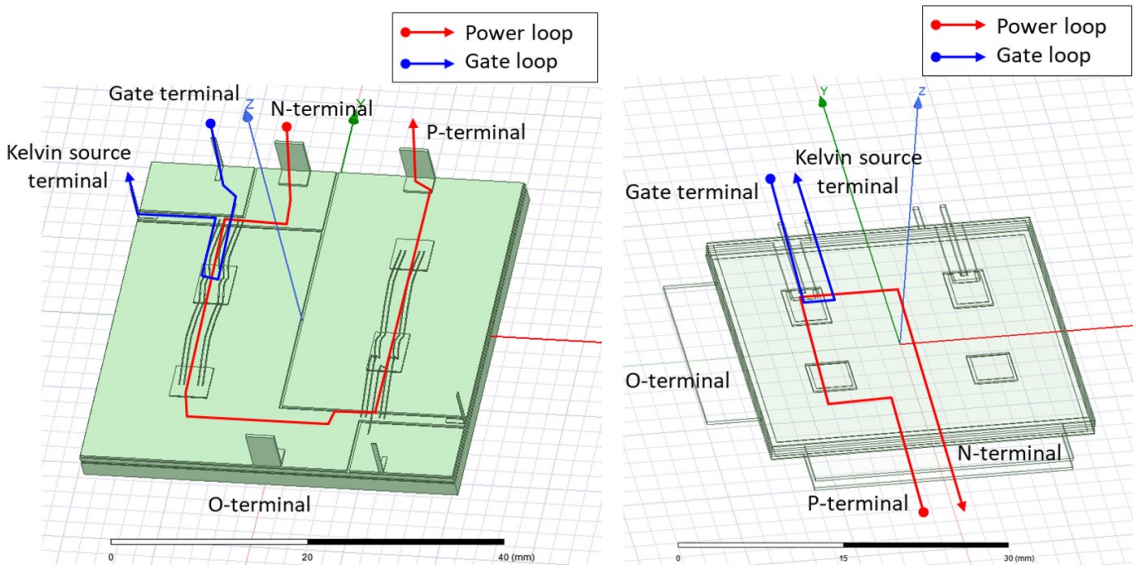


Figure 4.10: The impact of overlapping area between P-N terminals in combination with the number of paralleling devices per switch position on parasitic inductance of the module.

Based on the previous thermal simulations and parasitic inductance studies, 40mm$\times$40mm footprint for conventional module and 30mm$\times$30mm footprint for 3D stacked module with 100% overlap P-N terminal design were selected for further electrical comparison studies. The overall module designs with their parasitic power loop and gate loop inductances are indicated on them as depicted in Fig. 4.11. The results of parasitic inductance and resistance extraction at 50MHz is summarized in Table. 4.6.The power loop inductance of the 3D stacked module shows about 30 times smaller value compared to the 19.9nH of conventional module due to the advantages of overlapping P-N terminals of the 3D structure.



(a) (b)

Figure 4.11: (a) Simulated power and gate loops for conventional module, (b) simulated power and gate loops

Table 4.6: Summary of parasitic inductance and resistance results

	Conventional Module		3D Module	
@50MHz	Power loop	Gate loop	Power loop	Gate loop
L [nH]	19.9	17.8	0.6	4.2
R [mΩ]	151	183.6	0.006	26.6

The difference in package parasitic inductance affect the voltage and current waveforms during switching.Using the parasitic inductance and resistance values obtained from Table. 4.6, a double-pulse testing set-up was simulated through MATLAB Simulink to see the difference of switching waveforms between conventional and 3D stacked modules. The properties such as on-resistance and capacitances were modified from a default MOSFET model to mimic properties of a commercial SiC MOSFET [99]. An example of the double-pulse simulation set-up which includes the parasitics is shown in Fig. 4.12, and

the resulting waveforms such as gate pulse, drain-source voltage, and the drain current are shown in Fig. 4.13. The turn-off and turn-on waveforms of both conventional module and 3D stacked module are presented in Fig. 4.14(a),(b), and a magnified plot focusing on the voltage overshoot at turn-off is shown in Fig. 4.14(c). The results of switching waveforms clearly show the 3D stacked module would yield cleaner waveform, less resonance, less delay, and much smaller voltage overshoot compared to the conventional modules with higher parasitic inductance.

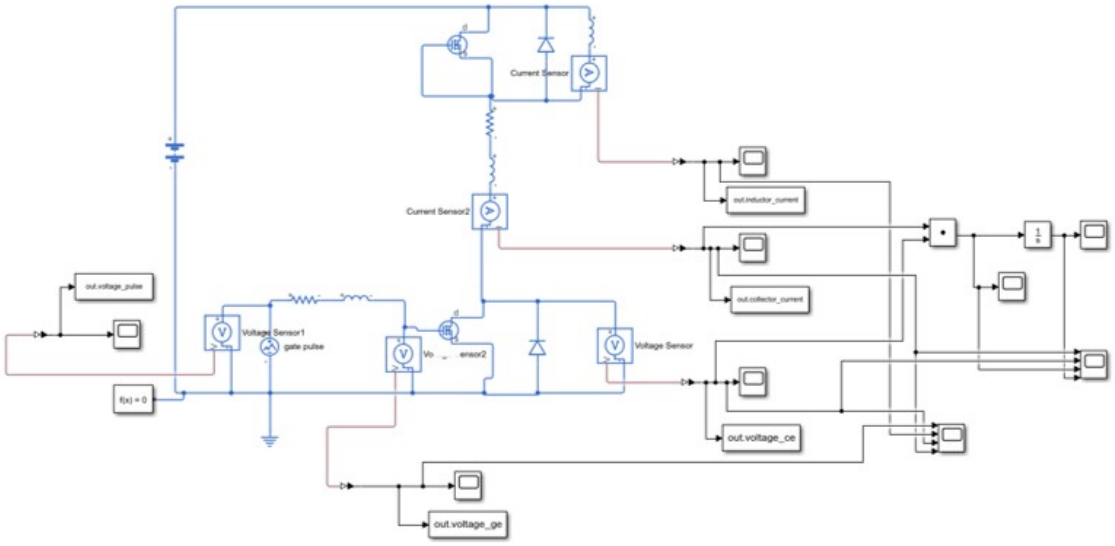


Figure 4.12: An example of double-pulse simulation set-up in MATLAB Simulink.

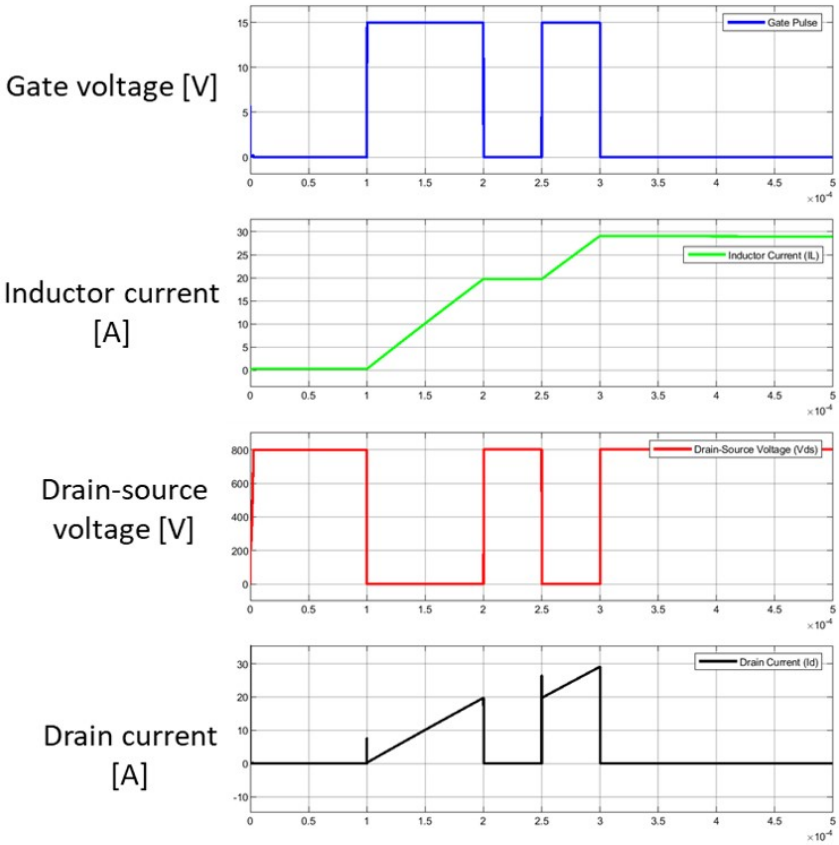


Figure 4.13: Switching waveforms as a result of double-pulse simulation. The gate pulses and corresponding voltage and current waveforms of the MOSFET are monitored.

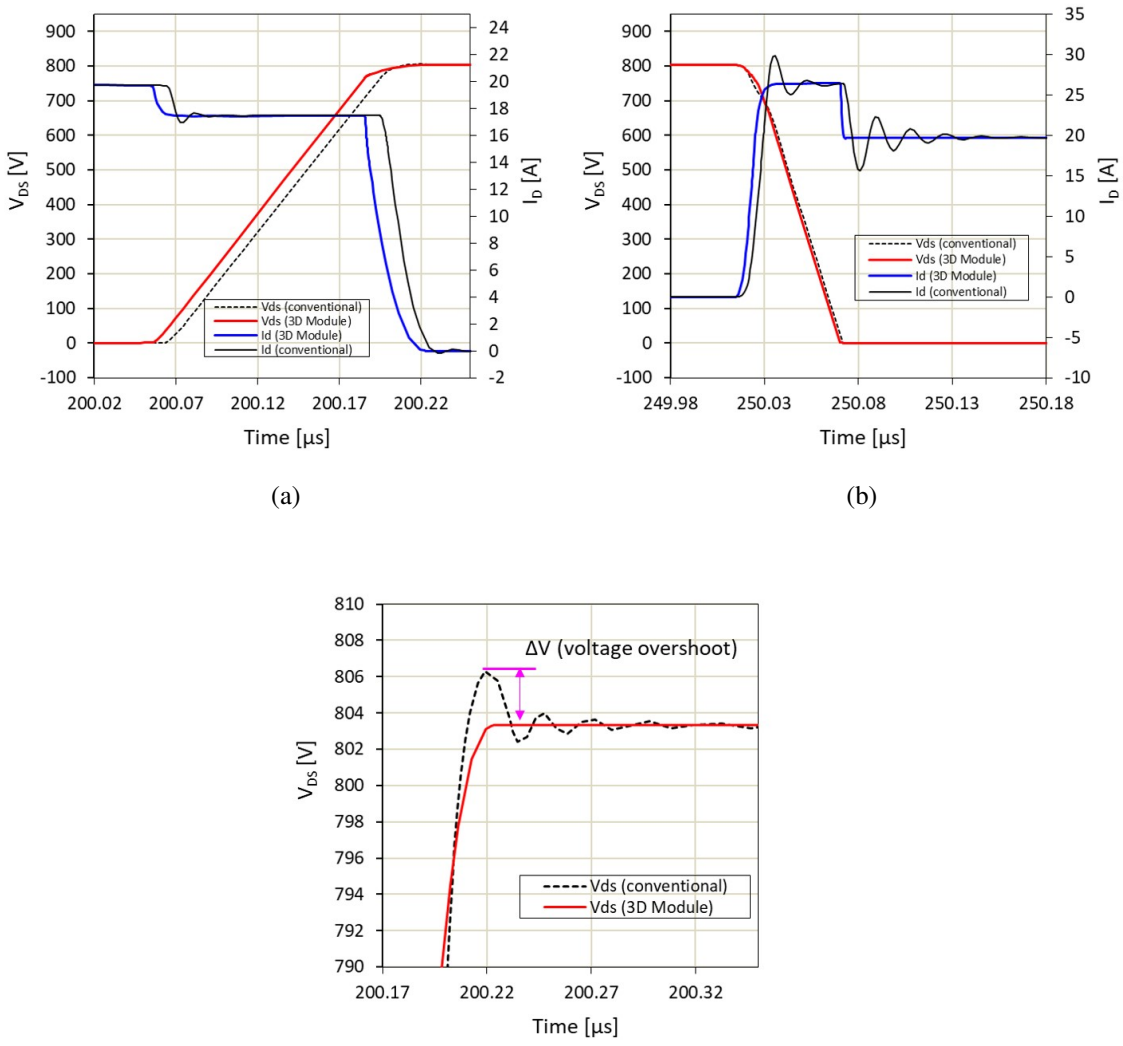


Figure 4.14: (a) Simulated turn-off switching waveform, (b) simulated turn-on switching waveform, (c)voltage overshoot at turn-off switching

The parasitic capacitances of the packages are also extracted from the models of conventional and 3D stacked module to assess their impact on common-mode noise. As shown in the simplified circuit schematic of the half-bridge module with a heatsink in Fig. 4.15, there exists parasitic capacitances from terminals to the heatsink. Among these various capacitances from terminal conductors to the heatsink, the parasitic capacitance from output

terminal to the heatsink (C^{out}) is the most significant one as it is acts as a main source for the common-mode noise current that flows to the cooling system. Using ANSYS Q3D, the parasitic capacitance from output terminal to heatsink (C^{out}) was extracted for both conventional and 3D stacked modules. The parasitic capacitances were 109pF and 1.3pF for conventional and 3D stacked modules, respectively, which is roughly two orders of magnitude difference. Relatively large capacitance of conventional module comes from the coupling between top metal trace and bottom metal plate of DBC substrate through ceramic dielectric layer. On the other hand, the output leadframe of 3D module does not have direct capacitive coupling to the heatsinks since it is situated in the middle between the top and bottom leadframes. The extracted capacitances were added to the output terminal in the MATLAB simulink simulation set-up from Fig. 4.12, and the time-domain current that flows through the parasitic capacitance were obtained as shown in Fig. 4.16. This simplification is to estimate and compare how much noise current would be generated from the parasitic capacitances of each conventional and 3D stacked modules. When dV/dt of the voltage at the output terminal was 5kV/μs, the peak amplitudes of the noise currents were 0.65A and 8.5mA for conventional and 3D stacked modules, respectively. Therefore, the 3D stacked module package with low-parasitic capacitance from output terminal to heatsink results in about 75 times lower noise current levels compared to the conventional module package.

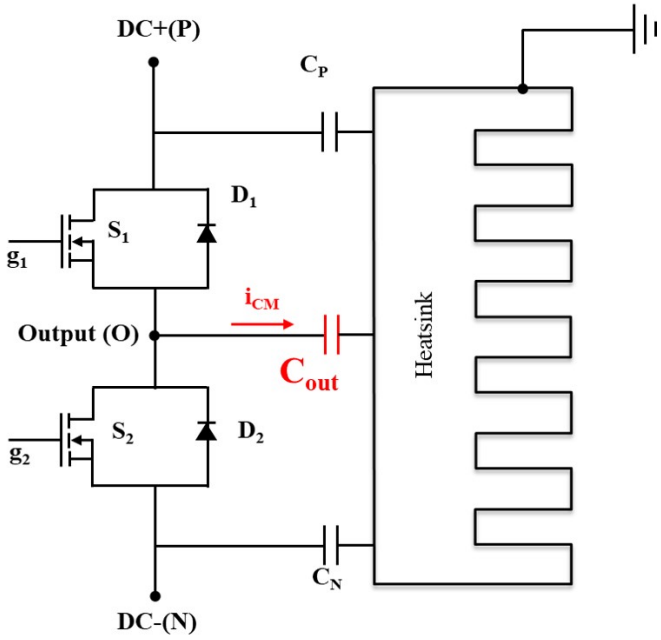
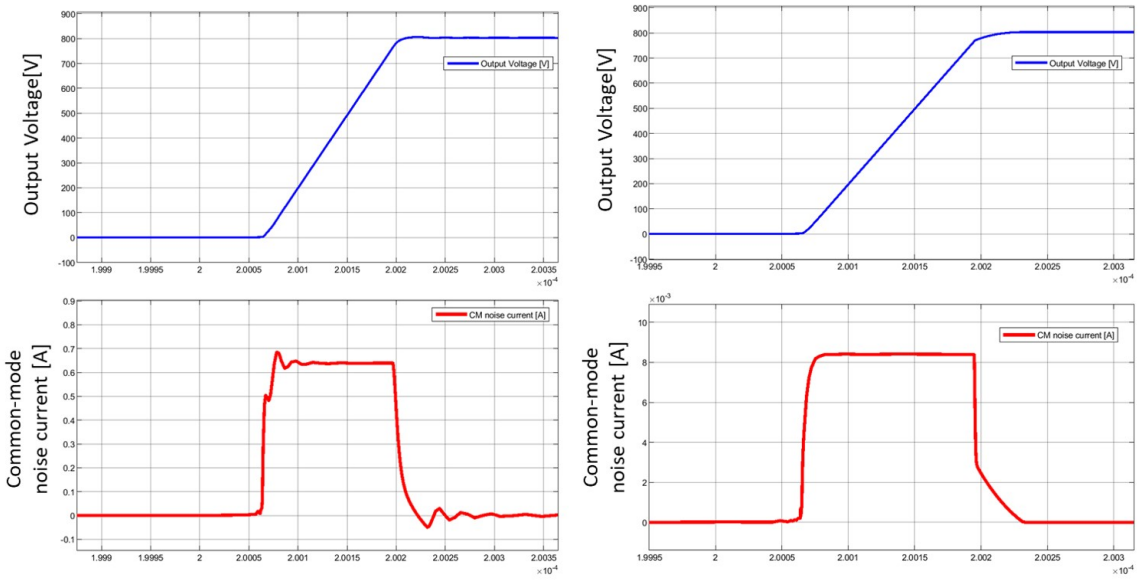


Figure 4.15: Switching waveforms as a result of double-pulse simulation. The gate pulses and corresponding voltage and current waveforms of the MOSFET are monitored.



(a) (b)

Figure 4.16: (a) Simulated common-mode current for conventional module, (b) Simulated common-mode current for 3D stacked module

CHAPTER 5

POWER MODULE DESIGN FOR SOFT-SWITCHING CONVERTERS

5.1 Current switch module for integrated motor drive application

An integration of electric motor and drive electronics as a single unit brings numerous advantages such as improved power density, reduced overall system cost, and improved electromagnetic interference (EMI) behavior [100]. This integrated motor drive (IMD) technology eliminates expensive and bulky components like shielded connection cables, a separate housing for the electronics, high-voltage and current bus bars, contributing to the reduction of the overall volume, weight, and cost of the combined system of motor and drive.

As IMD is a structural integration of motor with motor drive electronics, these two units are merged either in or on the same housing. Depending on the integration strategy, there are four principal configurations for IMDs: 1) the radial housing-mounted; 2) the axial housing-mounted; 3) the radial stator-mounted; 4) the axial stator-mounted as depicted in Fig. 5.1.

In the past, the motor and drive electronics were assembled in separate housings with wire harness connecting them. This approach had an advantage in flexibility to position the power electronics, however, the connection medium introduced additional signal noise by acting as an antenna [101]. Recently, it has become more common to integrate the motor and drive to achieve more compact and lightweight components with additional benefits of

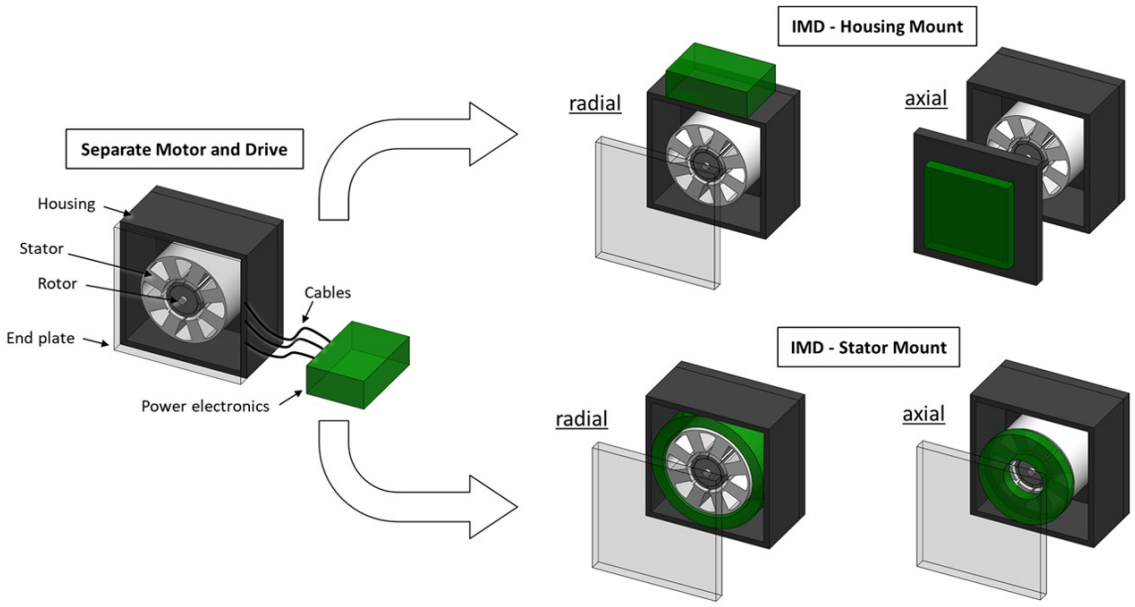


Figure 5.1: Different configurations for integrated motor and drive (IMD) technology.

reduced manufacturing cost, and reduced noise [101].

The integration of motor and drive not only have advantages, but also brings thermal challenges associated with this integration. Compared to the motor, the power converters have much higher power density with typical heat flux densities in the range of 50-200 W/cm^2, because of their high-power handling capabilities and relatively small volume [8]. These high heat concentrations from converter losses lead to complications in converter cooling and thermal management. In addition, integration of motor and drive for a single housing requires modification of layout or structure of the drive electronics. It is often required for the electronics to adjust their form factor to a curved surface or a circular board layout in order to enhance the compactness of the system.

Soft-switching converters are excellent candidates that can replace traditional inverter topology in IMD technology with potential advantages such as lower loss, smaller size, and less noise. For this specific application, a soft switching converter for IMD, a current switch

power module was designed and optimized. Key focuses of the design and optimization of the module were to yield smallest layout size at a given harsh thermal constraints, to have low parasitic inductance to prevent malfunctioning of the converter, and to have modular design to add flexibility in integration of the system.

5.2 Module design with focuses on package thermal and electrical characteristics

A simplified version of a overall structure of a soft-switching converter, developed by Center for Distributed Energy at Georgia Tech, is presented in Fig. 5.2 [102]. The converter is constructed with three main parts; DC input connected to the battery source, resonant network, and the 3 phase AC output to drive the motor. The purpose of this chapter is to design a power module that will be used as a single phase leg, or a half bridge structure for this converter. This converter requires sophisticated and accurate control scheme for operation utilizing the resonant network. Thus, the primary feature this novel module package should have is low inductance with symmetric layout. High parasitics as well as asymmetry in layout can cause distortion in accurate timing or imbalance in currents which might cause malfunction of the converter. Secondly, the package should be compact with a modular design so that it can easily be integrated with the motor. Thirdly, the package should be low thermal impedance compared to conventional approaches. The coolant in the cold plate for the power electronics is intended to be shared with the coolant of the motor, which imposes a stringent thermal conditions on the power module package. The novel power module package should address the challenges described above.A concept image of the overall soft switching converter for IMD application is shown in Fig. 5.3. The power modules are assembled on a cold plate (power stage), and the gate driver IC board (control

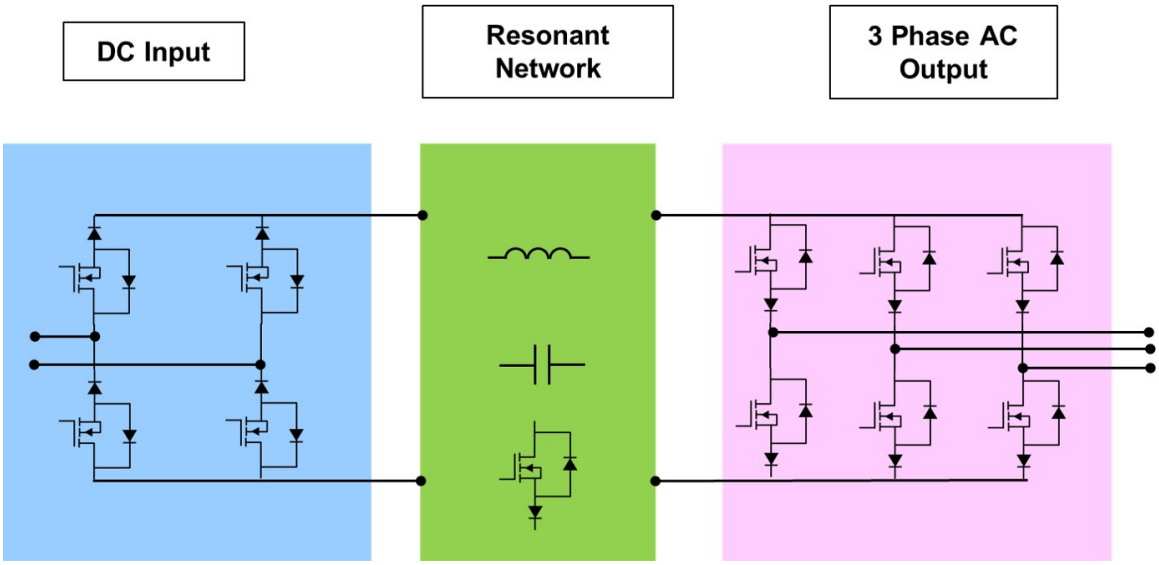


Figure 5.2: A simplified schematic of overall soft switching converter structure

stage) is placed on top of the power stage. The passives are integrated to either power stage or on top of the control stage, depending on their size and ratings.

The specifications of the converter are summarized in Table. 5.1. The devices were selected from commercially available SiC devices, which have low on-resistance, high current ratings, and voltage ratings higher than the DC bus voltage. The thermal boundaries of the cooling system is also presented in the Table. 5.1. The coolant temperature, heat transfer coefficient of the cold-plate, and the allowable maximum operating junction temperature of the SiC devices will determine how large the package layout should be and whether the materials and package layers are suitable for thermal dissipation. The number of devices used per switch position is determined based on the current rating of the converter, and considering the efficiency of the overall converter. Shown in Table. 5.2 is the selected device configuration (2 MOSFETs and 4 diodes), and estimated loss distribution of a switch position in worst case scenario (highest loss) of the converter operation.Given these thermal and electrical constraints, the objective of this design study was to estimate

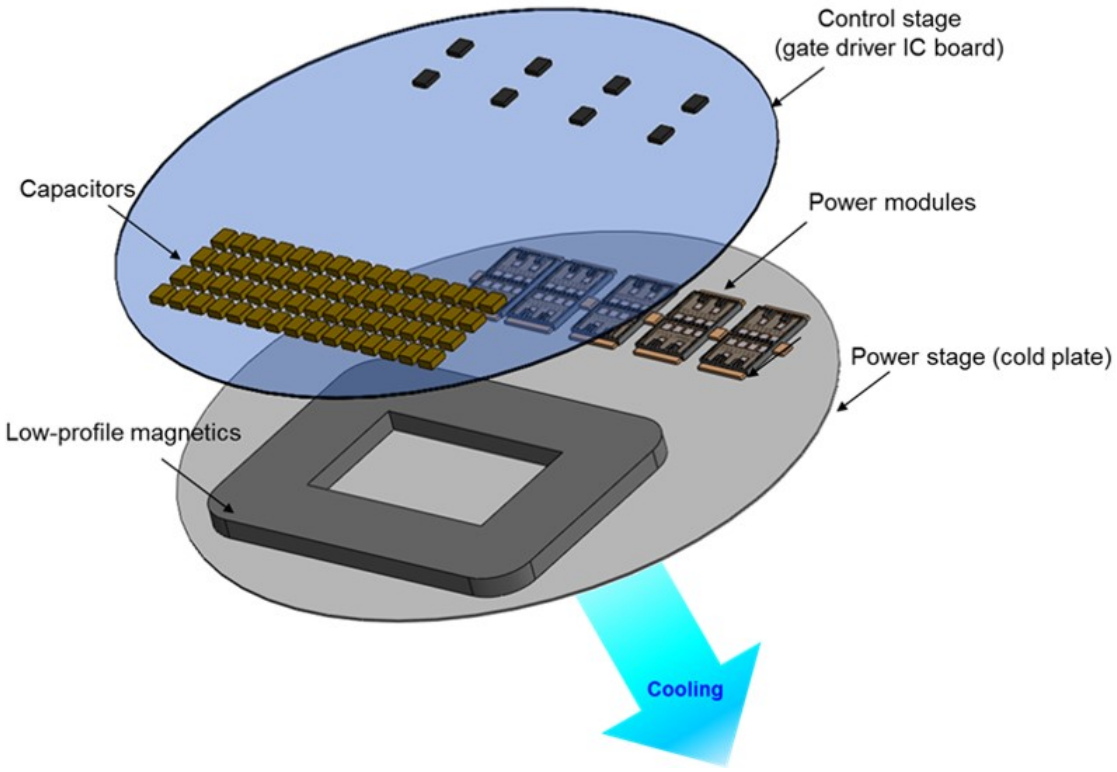


Figure 5.3: A concept image of overall converter structure with key components

appropriate module size that can result in maximum junction temperatures below 175°C for all the dies, and to have low inductance package that satisfies package internal separation distances that is sufficient enough to prevent any electrostatic failures.

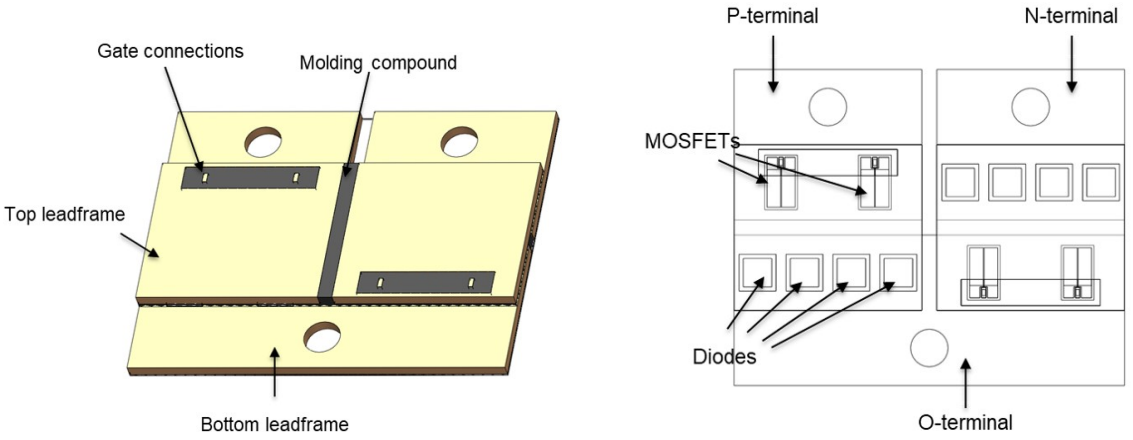
Based on semiconductor loss estimations of the converter, a baseline design of half-bridge multichip module package architecture integrating two SiC MOSFETs and four SiC

Table 5.1: Converter Specifications

Items	Specification
SiC MOSFET (Cree CPM3-1200-0013A)	1200V / 149A, Ron=13mΩ
SiC Diode (Cree CPW5-1200-Z050B)	1200V / 50A
VDC, IDC of converter	600 V / 120 A
Switching frequency	20 kHz
Coolant temperature	80°C
Heat transfer coefficient of cooling technology	10000 W/m^{2}K
Maximum junction temperature	$\leq$ 175°C

Table 5.2: Device Loss Estimations

Device	Total loss per switch position	# of dies	Loss per die	Die dimension	Loss density
Diode	208W	4	52W	4.9 mm×4.9mm×0.38 mm	5.7×10^9 W/m^3
MOSFET	155W	2	78W	4.36 mm×7.26 mm×0.18 mm	13.7×10^9 W/m^3



(a) (b)

Figure 5.4: Designed baseline module. (a) Overall module image, (b) transparent view of the module.

diodes was created as shown in Fig. 5.4. This module consists of upper and lower switches in a half-bridge configuration. To meet the desired module ratings, two MOSFETs and four diodes were paralleled for each switch position. The proposed package architecture is leadframe-based, eliminating the traditional thick DBC substrates and wire bonds by use of double-sided die-attach joints and insulating layers. The cross-section of the module and the layer thicknesses are shown in Fig. 5.5. The Ag sintering pastes will be used as the die attach materials, and the isolation film acts as insulator between the terminal and heatsink. The thickness of top and bottom leadframes were determined considering high current handling capability as well as the heat spreading effect.

The module size was increased from the baseline dimensions (52mm×42mm) to find the optimum width and length that satisfies the aforementioned thermal constraints. The

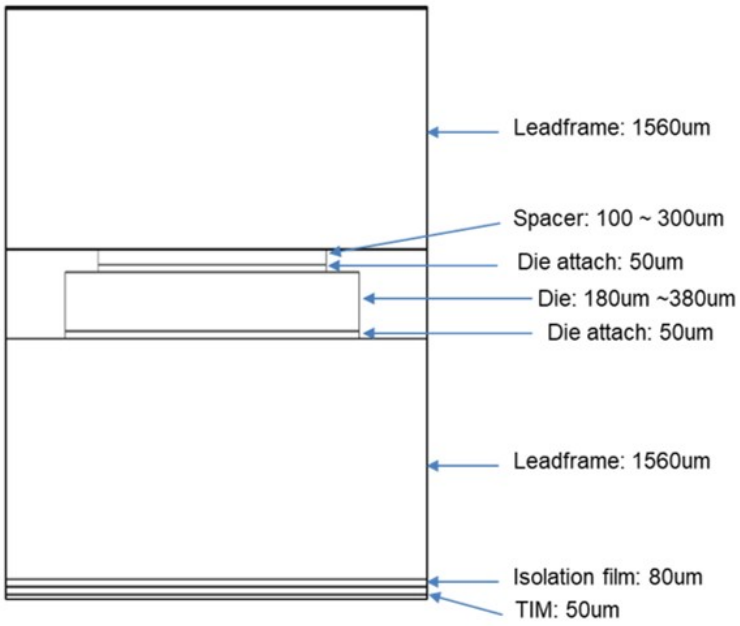


Figure 5.5: A cross-sectional image of the baseline module design

baseline dimensions were determined based on the smallest physical layout that could be assembled without considering the thermal conditions. Different dimensions of the modules that are simulated are shown in Table 5.3. The thickness of the modules remained the same for all the cases. Steady-state thermal simulations with these design cases were conducted using ANSYS Workbench. The bottom surface of the module was set to have a heat transfer coefficient of 10000 W/m^{2}K with an ambient temperature of 80^{o}C to represent the cold plate. On the other hand, the top surface of the module was set to have convective air cooling at 10 W/m^{2}K at 22^{o}C (natural air convection). The effect of the molding compound that fills the gap between the top and bottom leadframes was ignored to simplify the simulation process. The thermal conductivities of different package layers used in the simulation are presented in Talbe 5.4. As the SiC devices are vertically conducting devices, Volumetric heat densities of 13.7e9W/m^3 and 5.7e9W/m^3 were applied to MOSFETs and

Table 5.3: Different module sizes simulated

Case 1 (baseline)	**Case2**	**Case 3**	**Case 4**	**Case 5**
52mm×42mm	52mm×52mm	62mm×62mm	72mm×72mm	82mm×82mm

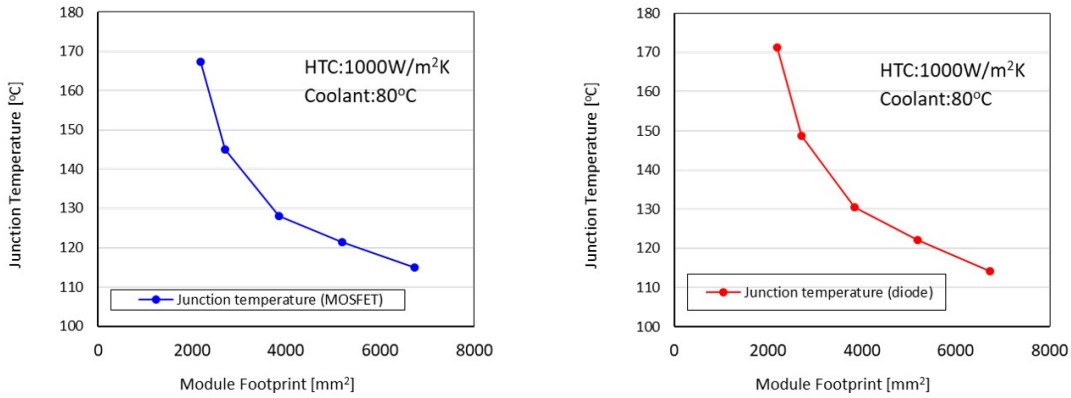
Table 5.4: Thermal conductivity values of components

Component	**Thermal Conductivity [W/mK]**
Leadframe (Cu)	400
Spacer (Cu)	400
Die attach (sintered Ag)	240
Die (SiC)	370
Isolation film (epoxy with filler)	3
TIM	3

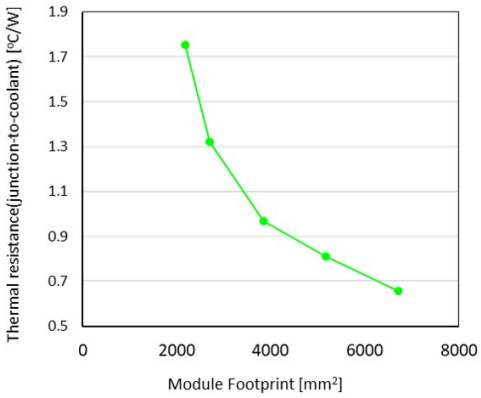
diodes, respectively.

The resulting junction temperature values for MOSFET and diode at the given thermal boundaries are shown in Fig. 5.6(a)-(b). The junction temperatures in both MOSFETs and diodes showed a significant decrease as the footprint increased. The junction temperatures of diodes showed higher values compared to the MOSFETS, indicating the temperature of the diodes is the limiting factor when we want to obtain the smallest footprint. From the plot of Fig. 5.6(b), the junction temperatures of all the footprints simulated fall below 175°C. Thus, the smallest footprint that can be achieved with junction temperature less than 175°C is 52mm×42mm (baseline). In order to see how increasing the footprint affects the package thermal resistance of the module, the thermal resistance from a diode to coolant (junction-to-coolant) was calculated in Fig. 5.6(c).

Although the values were fixed in the previous simulations, the cooling conditions (heat transfer coefficient and coolant temperature) for the module have an important role in determining the junction temperature as well as the footprint size. In order to examine how those parameters impact the junction temperature and resulting footprint, additional simulations



(a) (b)

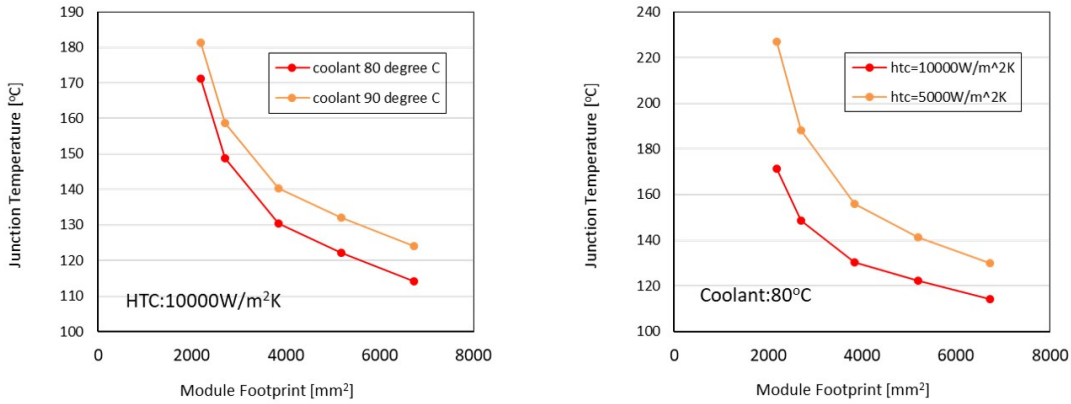


(c)

Figure 5.6: Thermal simulation results with increasing module sizes. (a)Junction temperature for MOSFETs, (b) junction temperature for diodes, (c) junction-to-coolant thermal resistance for a diode.

were conducted with heat transfer coefficient of 5000W/m^{2}K, and coolant temperature of 90^{o}C. Both plots in Fig. 5.7(a)(b) suggests that decreasing the heat transfer coefficient or increasing the coolant temperature have adverse effects in the junction temperatures by shifting the curves upwards. Therefore, it is important to set the heat transfer coefficient as high as possible, while maintaining the coolant temperature as low as possible to achieve smallest footprint of the module.

In real operation of the converters, the coolant temperature as well as the heat trans-



(a) (b)

Figure 5.7: Thermal simulation results with different cooling conditions. (a)Junction temperature of diode with different coolant temperature, (b) junction temperature of a diode with different heat transfer coefficient.

fer coefficients can vary. Thus, it is critical to have some margin in the module design, so that even in the worst and unexpected cases the device would still not fail to operate within the package without exceeding the maximum allowable junction temperature. Additional modifications from the baseline module was conducted to explore possibilities to reduce the junction temperature further. Two variations (option B, option C) from the baseline design (option A) were created as shown in Fig. 5.8. Option B changes the interface between the bottom leadframe to the heatsink from encapsulant film and TIM (thermal interface material) to a ceramic insulator and TIMs. Instead of the encapsulant film (80μm)-TIM(50μm) combination, the insulation layer in option B consists of Solder(40μm)-AlN(200μm)-TIM(20μm). Option C rearranges the diodes from option B into a 2 by 2 array instead of 1 by 4 array. This rearrangement seeks to save the space in the horizontal direction, and distributes heat more evenly. The junction temperatures of each variations as well as the calculated thermal resistances from junction-to-coolant are

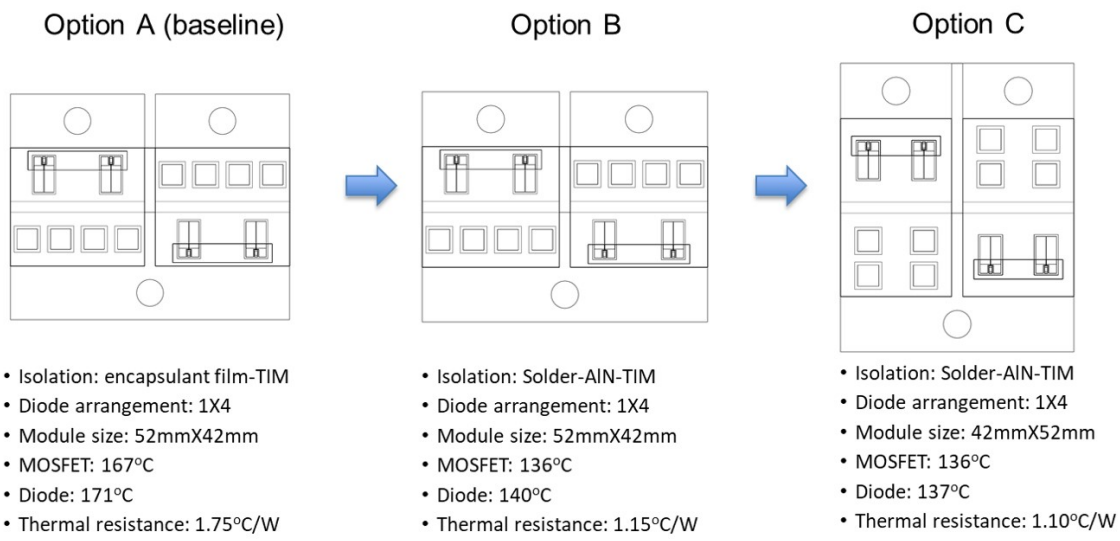


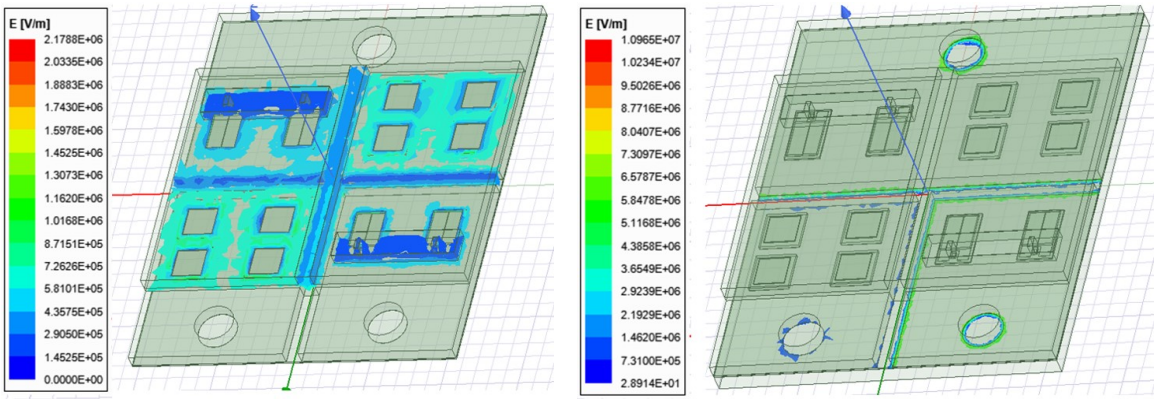
Figure 5.8: Different variations from the baseline module

shown in Fig. 5.8. A significant improvement in thermal resistance and reduction in junction temperature could be achieved by modifying the isolation interface and rearrangement of the diodes. The option C was selected as a final design as it showed the lowest junction temperature as well as the lowest thermal resistance in a given footprint.

With the finalized module design an electrostatic analysis was conducted using ANSYS Maxwell to verify if the module package can safely handle the voltage difference of the converter which is 600V. Electric field within the module was simulated when voltage was applied to terminals based on several different modes of operation. To have sufficient margin and ensure safety, the voltage of 1200V, instead of 600V, was applied to terminals between P-to-N, P-to-O, top leadframe-to-O. The maximum electric field within dielectric materials were monitored to see if the insulation materials and separation between the terminals meet proper isolation requirements. The dielectric strength of insulation materials, and the resulting maximum electric field (only the highest values in different operating modes) are summarized in Table. 5.5. These results suggest that all the materials and

Table 5.5: Maximum magnitude of electric field in dielectric materials at 1200V

Material	**Dielectric constant**	Max E-field (magnitude)	Dielectric strength
Molding compound	3.6	9.5 MV/m	20 MV/m
Ceramic (AlN)	8.8	11.0 MV/m	14 MV/m
TIM	6.7	8.8 MV/m	15MV/m



(a) (b)

Figure 5.9: Results of electrostatic simulation in ANSYS Maxwell. (a)Electric field distribution of molding compound when 1200V was applied across P-N terminals, (b) electric field distribution of ceramic layer when 1200V was applied across bottom leadframes to heatsink.

distances between conductors satisfies the isolation requirements even in elevated voltage levels. Examples of electric field (magnitude) distribution to visualize the highest field concentration, are presented in Fig. 5.9.

In order to assess the parasitic inductance of the finalized package design, ANSYS Q3D was utilize. The internal package parasitic inductances across different terminals were simulated and summarized in Talbe. 5.6. The inductances between P-to-N terminals, and P-to-O terminals were simulated for the main power loop. P-to-N terminals show lower inductance as the terminals are oriented side-by-side with flat conductors, which allows some magnetic field cancellation. Symmetric and low gate loops inductances are critical in accurate timing and control of the paralleled MOSFET devices. For that reason,

Table 5.6: Parasitic inductances and resistances extracted from ANSYS Q3D at 50MHz

Path	Inductance [nH]	Resistance (AC)[mohm]
P-O terminal	18.2	4.9
P-N terminal	9.8	13.1
Gate-Kelvin 1	8.1	30.1
Gate-Kelvin 2	8.1	30.5

a gate connection board was designed to integrate the gate drivers and controllers in close proximity in the vertical direction with a focuses on symmetry of the layout as shown in Fig. 5.10. Gate loop inductances for each paralleled MOSFETs show that the values are almost identical without any discrepancies.As the layout for the power loop is also symmetric, and as the devices are positioned with equal spacings, no signficant deviation in inductances for current paths of individual MOSFETs were oberved, which indicates there would be uniform current distribution during conduction.

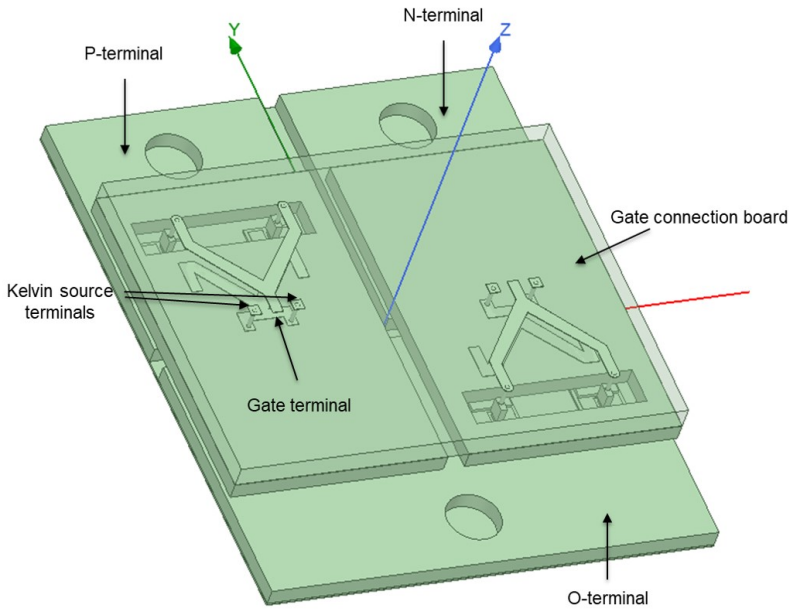


Figure 5.10: Power module with gate connection board

The designed power module package is compared with conventional packaging ap-

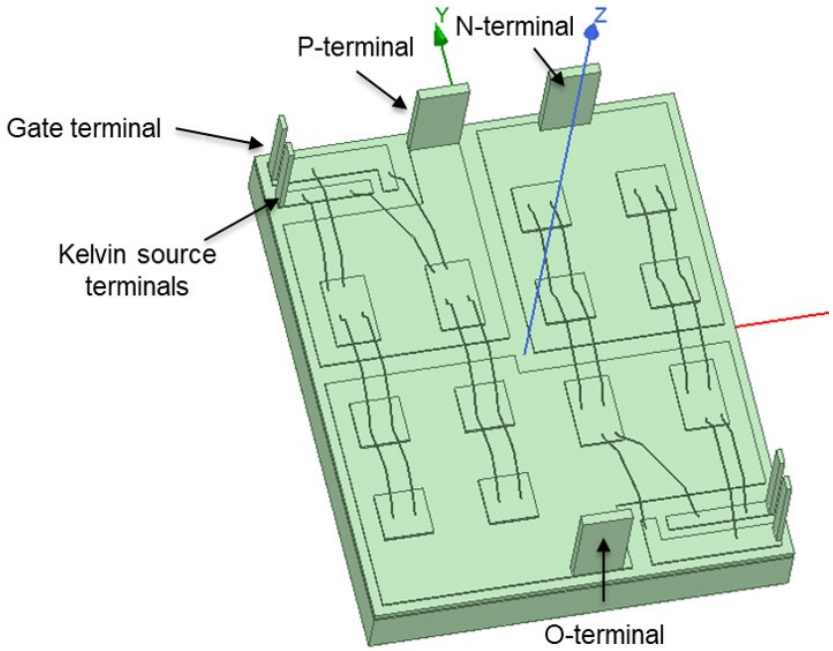


Figure 5.11: Power module with conventional packaging approach

proach to see the improvement in thermal resistance and electrical parasitics aspects. The conventional approach uses DBC substrate with Aluminum wirebonds for devices' top-side interconnection. The interface between bottom-side of DBC and cold plate consists of solder-baseplate(AlSiC)-TIM, and the module footprint size(42mm$\times$52mm) is kept the same as the leadframe-based power card approach. The designed module package using DBC and wirebond based conventional structure are shown in Fig. 5.11. The key thermal and electrical specifications of the two packaging approaches are compared in Table. 5.7 and Table. 5.8, respectively. The thermal and electrical simulation set-ups were the same as the conditions used for the leadframe-based power card approach. In the comparison of the thermal simulation results indicate that leadframe-based power card approach has lower junction temperatures and thermal resistance values at a given footprint. This advantages are due to simplified and thin package layers from the bottom side of the module to the

Table 5.7: Thermal comparison for leadframe-based power card and conventional approaches

HTC = 10kW/m^{2}K, Coolant=80^{o}C	**Power Card**	**Conventional**
Junction temperature (MOSFET)	136^{o}C	166^{o}C
Junction temperature (diode)	137^{o}C	141^{o}C
Thermal resistance (junction-to-coolant)	1.1^{o}C/W	1.2^{o}C/W
Module size	42mm$\times$52mm$\times$6mm	42mm$\times$52mm$\times$13mm

Table 5.8: Electrical parasitics comparison for leadframe-based power card and conventional approaches

	Power Card		**Conventional**	
	Inductance [nH]	**Resistance [mohm]**	**Inductance [nH]**	**Resistance [mohm]**
P-O terminal	18.2	4.9	26.5	45
P-N terminal	9.8	13.1	19.5	82
Gate-Kelvin 1	8.1	30.1	25.7	245
Gate-Kelvin 2	8.1	30.5	29.7	244

cold plate. In addition, the module size comparison shows that power card approach will have around two-fold increase in the power density per module.

The electrical parasitic comparison in Table. 5.8 shows the leadframe-based power card approach's superiority in low and symmetric inductance package. For example, the parasitic inductance between P-O terminals is 30% lower in the power card approach compared to the inductance of the conventional approach. This low value is attributed to the flat leadframe conductors on the topside interconnection instead of lengthy wirebonds with high loop heights. The gate loop inductances are about 3 times lower in power card approach compared to the gate loop inductances of conventional approach as the gate board is directly integrated on the top-side of the module with symmetrically designed gate connections. The standard deviation of gate loop inductances are 0 and 2 for power card and conventional approaches, respectively, indicating the power card approach would be much reliable in accurate switch timings.

In this chapter, a novel package design for current switch module packages was carried out. The design emphasis of the proposed power module was determined based on the unique packaging requirements that arise from the unconventional device configuration of current switch modules and the environment of this specific integrated motor drive system. A leadframe-based power card design was analyzed to determine the optimum module footprint to meet the thermal constraints, and the finalized design was simulated to study the electrostatic and parasitic characteristics of the package. Finally, the proposed power card approach is compared with the conventional power module packaging approach to verify improvements in thermal, electrical, and size aspects. In this comparison, the proposed design showed 8.3% reduction in thermal resistance, 30% reduction in parasitic inductance, and 50% reduction in module volume compared to the conventional package design. These accomplishments successfully addressed the design challenges associated with current switch modules for integrated motor drive applications.

CHAPTER 6

SUMMARY AND CONCLUSION

The objectives of this research were to design and demonstrate novel power module packaging for SiC devices. There were numerous challenges associated with SiC power module packaging technologies including, switching waveform distortion (overshoot and resonance) by parasitic inductance, high-level of noise generated from increased dv/dt and parasitic capacitance, and high-thermal densities that could potentially aggravate package reliability. In order to address these challenges, a leadframe based 3D stacked power SiC power module was designed and demonstrated.

6.1 Research summary

6.1.1 Design and demonstration of full-bridge rectifier module

The focus of this study is to design and demonstrate a 3D power module package with reduced parasitics and low thermal resistance, through a vertically-stacked structure. A full bridge rectifier (FBR) configuration was selected as a first test-vehicle implementation to showcase the benefits of the proposed 3D power packaging approach in achieving superior electrical and thermal characteristics that are benchmarked against wire-bonded conventional packaging. The simulation results of the proposed 3D approach show a 40% reduction in parasitic inductances, more than 10 times reduction in parasitic capacitances, and 2 times reduction in junction-to-case thermal resistance of the package as compared to

the conventional reference design. A manufacturing process, including the process design, materials selection, and development of unit processes, was established. They were applied to fabricating FBR prototypes with active diodes which were then tested for functionality. Measurements of the parasitics inductance(L), parasitic capacitance(C), and thermal resistance were carried out on specifically designed test vehicles, confirming simulations and modeling with the measurements of the fabricated modules.

6.1.2 Design and modeling for half-bridge module

In this study, a 3D stacked package design for half-bridge module was studied to achieve low-parasitics, and enhanced thermal performance than the conventional packaging approaches. A half-bridge module package was first thermally designed with its layout and size to meet power module specifications for EV applications. Secondly, the parasitic inductance was studied with different parametric designs to determine the impact of terminal designs to the extracted parasitic inductance. From these design studies, reference models were designed in parallel for comparison with conventional packaging approaches.

Given the same thermal boundary conditions, the 3D stacked module required smaller module footprint area to dissipate the heat generated from the devices, compared to the conventional modules. The comparison in thermal Resistance values showed that the 3D stacked module had about 18% reduction in thermal resistance (junction-to-coolant) compared to the conventional module at the same module size of 40mm$\times$40mm.

Parametric studies on various terminal designs were carried out to identify which module design feature critically affected the parasitic inductance of the power loop. Compared to baseline designs where the terminals are arranged side-by-side, module designs with

overlapping P-N terminals turned out to reduce the inductance significantly, from 15nH to 0.6nH. With the extracted parasitic inductance and resistance, a double-pulse testing was simulated using MATLAB Simulink. The results of switching waveforms showed that the 3D stacked module yielded cleaner waveform, less resonance, less delay, and much smaller voltage overshoot compared to the conventional modules with higher parasitic inductance. The parasitic capacitances of the packages are also extracted from the models of conventional VS. 3D stacked module to assess their impact on common-mode noise. When dv/dt at the output terminal was 5kV/μs, the peak amplitudes of the noise currents were 0.65A and 8.5mA for conventional and 3D stacked modules, respectively.

6.1.3 Power Module Design for Soft-Switching Converters

In this study, a current switch module package, for a soft switching converter, developed by Center for Distributed Energy at Georgia Tech, was designed. The design emphasis of the proposed power module was determined based on the unique packaging requirements that are specific for an integrated motor drive application. A leadframe-based power card design was analyzed to determine the optimum module footprint to meet the thermal constraints, and the finalized design was then simulated to study the electrostatic and parasitic characteristics of this package. A gate connection board was then designed to make sure the paralleled devices were laid out with symmetry to prevent difference in switch timings of the devices. Finally, the proposed power card approach is compared with the conventional power module packaging approaches to verify improvements in thermal, electrical, and size aspects. In this comparison, the proposed design showed 8.3% reduction in thermal resistance, 30% reduction in parasitic inductance, and 50% reduction in module volume

compared to the conventional package designs. These accomplishments successfully addressed the design challenges associated with current switch modules for integrated motor drive applications.

6.2 Conclusion

A novel way of packaging power modules in a 3D stacked architecture was proposed and demonstrated in this research. Unlike previously demonstrated 3D packaging proof-of-concept test vehicles using lab-scale manufacturing processes [15, 50, 51, 52, 53], this approach, based on leadframe-type substrates, is highly modular and compatible with current and future manufacturing infrastructures. The research led to a compact 3D stacked package with large-area of sintered joints, on both sides of the power devices. This unique structure has the flexibility to incorporate different geometries and materials for heat spreaders and isolation layers thus, enabling precise control of critical multi-physics design parameters such as parasitic capacitances and thermal resistances, in addition to allowing for ease of scalability to higher power ranges. Moreover, the suggested approach eliminates unnecessary structures or complex fabrication processes such as via drilling, thus making it suitable for a high volume manufacturing process for low-cost.

6.3 Recommendations for future work

As the development of power electronics using SiC devices head towards higher voltage and current rating, in smaller volume, the thermal, mechanical, and electrical requirements for the power module packaging technology becomes more stringent. Thus, advanced designs, materials and assembly technologies of power module need to be explored. To better

understand and satisfy the future demands, the following research areas are recommended for high-temperature, high-reliability, and high-speed switching power module packages.

1) Identifying new materials, such as encapsulants and die attach materials, for higher temperature operation and their long-term HT stability.

2) Advanced die-attach and bonding technologies that result in reduced stresses are required. This requires the CTE of materials in the package layers to be matched as best as possible in order to minimize the stress.

4) Alternatives to gate drive and passive components that can withstand and show minimal performance degradation at temperatures above 200^{o}C are required. This will allow higher-level of integration, thereby, enabling more compact and highly efficient packages.

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